PCI Express®
Mini Card Electromechanical Specification
Revision 2.1

~~November 21~~December 9, 2016

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2.1	Incorporated the following: • Add ~~USB 3.0~~USB3.1 to the Mini Card • Tighten Mini Card Power Rail Voltage Tolerance • Change Min value in Table 3-9~~Table 3-9~~ for +3.3 Vaux from 3.3 – 9% to 3.3 – -5% • ECN_L1_PM_Substates_with_CLKREQ_31_May_2013 • PCIe-MiniCEM-Combined-Antenna-Tuning-Coexistence_Signals_ECN_May_31_2012 • PCIe_Base_r3_0_Errata_2014-10-23 • Misc changes from MiniCard_2.1_errata_table • MiniCard_2.1 Errata Table, November 14, 2016 • Updated for USB3.1 Gen1 • Updated Figure 1-2, Logical Representation of the PCI Express Mini Card Specification	12/09/2016~~21~~

Membership Services

www.pcisig.com

E-mail: administration@pcisig.com

Phone: 503-619-0569

Fax: 503-644-6708

Technical Support

techsupp@pcisig.com

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1

1. Introduction

1.1. Overview

This specification defines an implementation for small form factor PCI Express cards. The specification uses a qualified subset of the same signal protocol, electrical definitions, and configuration definitions as the *PCI Express Base Specification, Revision 2.0*. Where this specification does not explicitly define PCI Express characteristics, the *PCI Express Base Specification* governs.

The primary differences between a PCI Express add-in card (as defined by the *PCI Express Card Electromechanical Specification*) and a PCI Express Mini Card add-in card is a unique card form factor optimized for mobile computing platforms and a card-system interconnection optimized for communication applications. Specifically, PCI Express Mini Card add-in cards are smaller and have smaller connectors than standard PCI Express add-in cards.

Figure 1-1~~Figure 1-1~~ shows a conceptual drawing of this form factor as it may be installed in a mobile platform. Figure 1-1~~Figure 1-1~~ does not reflect the actual dimensions and physical characteristics as those details are specified elsewhere in this specification. However, it is representative of the general concept of this specification to use a single system connector to support all necessary system interfaces by means of a common edge connector. Communications media interfaces may be provided via separate I/O connectors and RF connectors each with independent cables as illustrated in Figure 1-1~~Figure 1-1~~.

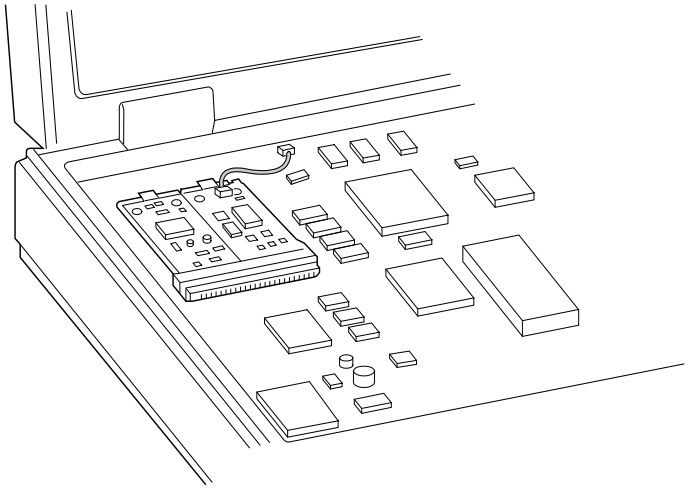


Figure 1-1: PCI Express Mini Card Add-in Card Installed in a Mobile Platform

PCI Express Mini Card supports two primary system bus interfaces: PCI Express and USB as shown in Figure 1-2~~Figure 1-2~~.

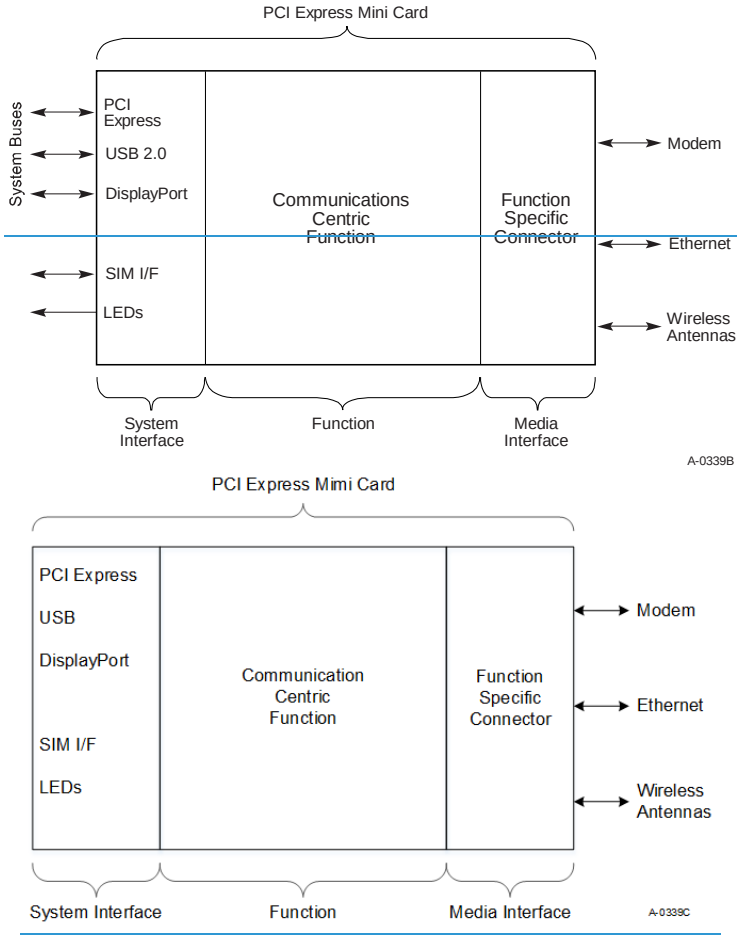


Figure 1-2: Logical Representation of the PCI Express Mini Card Specification

1.2. Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

- *PCI Express Base Specification, Revision ~~2.0~~3.1*
- *PCI Express Card Electromechanical Specification, Revision ~~2.0~~3.0*
- *PCI Local Bus Specification, Revision ~~2.3~~3.0*
- *Mini PCI Specification, Revision 1.0*
- *PCI Bus Power Management Interface Specification, Revision 1.2*
- *Advanced Configuration and Power Interface Specification, Revision ~~2.0b~~6.1*
- ~~*Universal Serial Bus 3.0 Specification, Revision 2.0*~~*USB2.0 - Universal Serial Bus Specification,* Revision 2.0, plus ECN and Errata, July 14, 2011, available from http://www.usb.org
- ~~*Universal Serial Bus Specification, Revision 2~~3.0~~1~~ *USB3.1 - Universal Serial Bus Specification,* Revision 3.1, plus ECN and Errata, July 14, 2011, available from http://www.usb.org
- *DisplayPort Specification, Revision ~~1.1a~~1.4*
- *SMBus Specification, Revision 2.0*
- *ELA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications*
- *ELA-364: Electrical Connector/Socket Test Procedures Including Environmental Classifications*
- *IS0/IEC 7816-2, 2007, Identification Cards – Integrated Circuit Cards – Part 2: Cards with Contacts – Dimensions and Location of the Contacts*
- *IS0/IEC 7816-3, 2006, Identification Cards – Integrated Circuit Cards – Part 3: Cards with Contacts – Electrical Interface and Transmission Protocols*

1.3. Targeted Applications

Although the PCI Express Mini Card is originally intended for both wired and wireless communication applications, it is not limited to such applications. Communications-specific applications may include:

Wired data communication:

- Local Area Network (LAN): 10/100/1000 Mbps Ethernet
- Wide Area Network (WAN): V.90/V.92 modem

Wireless data communication:

- Wireless-LAN (W-LAN): 802.11b/g/a (2.4 GHz and 5.2 GHz bands)
- Wireless-WAN (W-WAN): Cellular data (e.g., GSM/GPRS, UMTS, and CDMA-2000)
- Wireless-Personal Area Network (W-PAN): Bluetooth

The PCI Express Mini Card is targeted toward addressing system manufacturers' needs for build-to-order and configure-to-order rather than providing a general end-user-replaceable module. In specific applications, such as wireless, there are worldwide regulatory implications in providing end-user access to items such as antenna connections and frequency-determining components. It is up to the system manufacturer to limit access to appropriate trained service personnel and provide such notification to the user.

Although not specifically considered, other applications that may also find their way to this form factor include advanced wired WAN technologies (xDSL and cable modem), location services using GPS, and audio functions.

1.4. Features and Benefits

The performance characteristics of PCI Express make PCI Express Mini Card add-in cards desirable in a wide range of mobile systems. This mobile computer optimized form factor provides several benefits, including:

- **Upgradeability** – PCI Express Mini Card add-in cards are removable and upgradeable with available "new technology" cards. This allows upgrades to the newest technologies. System manufacturers are responsible for providing sufficient notification in the accompanying manual when a qualified technician should perform the upgrade service.
- **Flexibility** – A single PCI Express Mini Card interface can accommodate various types of communications devices. Therefore, the OEM manufacturer can supply build-to-order systems (for example, a network interface card instead of a modem or Token Ring instead of Ethernet).
- **Reduced Cost** – A standard form factor for small form factor add-in cards makes them more manufacturable, which may lead to reduced costs and provide an economy-of-scale advantage over custom manufactured form factors.
- **Serviceability** – PCI Express Mini Card add-in cards can be removed and easily serviced if they fail.
- **Reliability** – PCI Express Mini Card add-in cards will be mass-produced cards with higher quality than low-volume custom boards.
- **Software Compatibility** – PCI Express Mini Card add-in cards are intended to be fully compatible with software drivers and applications that will be developed for standard PCI Express add-in cards.
- **Reduced Size** – PCI Express Mini Card add-in cards are smaller than PC Cards, PCI Express add-in cards, Mini PCI add-in cards, and other add-in card form factors. This reduced size permits a higher level of integration of data communications devices into notebook PCs.
- **Regulatory Agency Accepted Form Factor** – Standardization of the PCI Express Mini Card form factor will permit world wide regulatory agencies to approve PCI Express Mini Card communications devices independent of the system. This significantly reduces cost and risk on the part of systems manufacturers.
- **Power Management** – PCI Express Mini Card is designed to be truly mobile friendly for current and future mobile specific power management features.

2

2. Mechanical Specification

2.1. Overview

This specification defines three small form factor cards for systems in which a PCI Express add-in card cannot be used due to mechanical system design constraints. These smaller cards are based on card-edge type connectors for system interfaces. Two PCI Express Mini Card system board connectors (52-pin and 76-pin) are defined.

In this document, *Mini Card* refers to all form factors. The three defined form factors will be individually identified as the *Full-Mini Card*, the *Half-Mini Card*, and the *Display-Mini Card* for the full length, half-length, and wider versions of the cards, respectively. The pin counts and system interfaces supported by each form factor are summarized in Table 2-1.

Table 2-1: Mini Card Form Factors

Card Type	Pin Count	PCI Express	USB	DisplayPort
Full-Mini Card	52	✓	✓	
Half-Mini Card	52	✓	✓	
Display-Mini Card	76	✓	✓	✓

2.2. Card Specifications

There are three PCI Express Mini Card add-in card sizes: Full-Mini Card, Half-Mini Card, and Display-Mini Card.

For purposes of the drawings in this specification, the following notes apply:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ± 0.15 mm, unless otherwise specified.
- Dimensions marked with an asterisk (*) are overall envelope dimensions and include space allowances for insulation to comply with regulatory and safety requirements.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.

2.2.1. Card Form Factor

The figures in this section illustrate example applications for the specified card form factors. The hatched areas shown in these figures represent the available component volume for the card's circuitry.

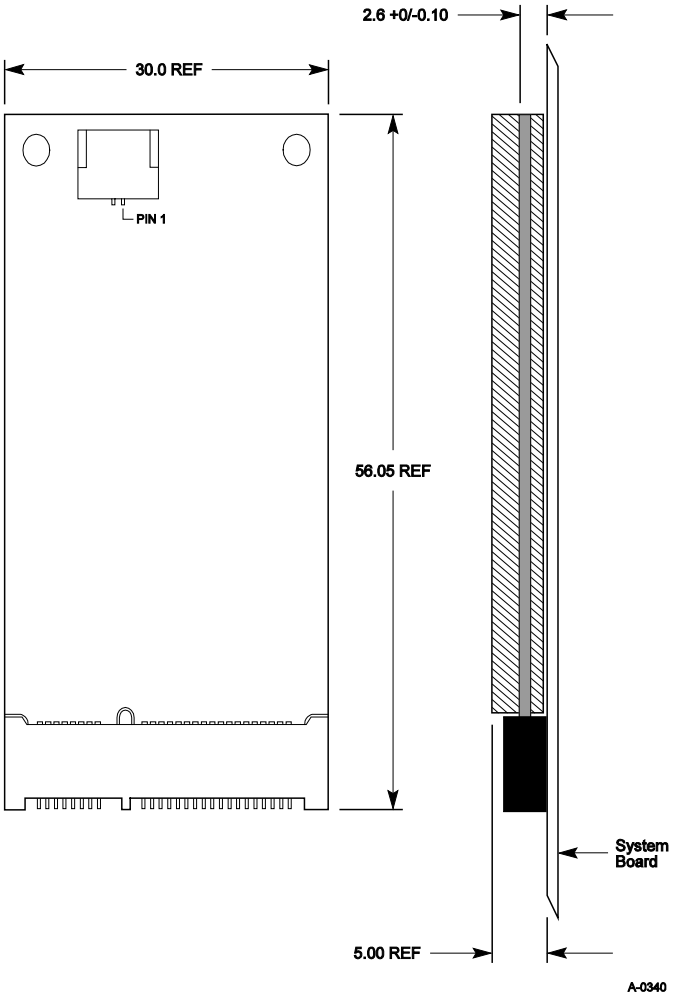


Figure 2-1: Full-Mini Card Form Factor (Modem Example Application Shown)

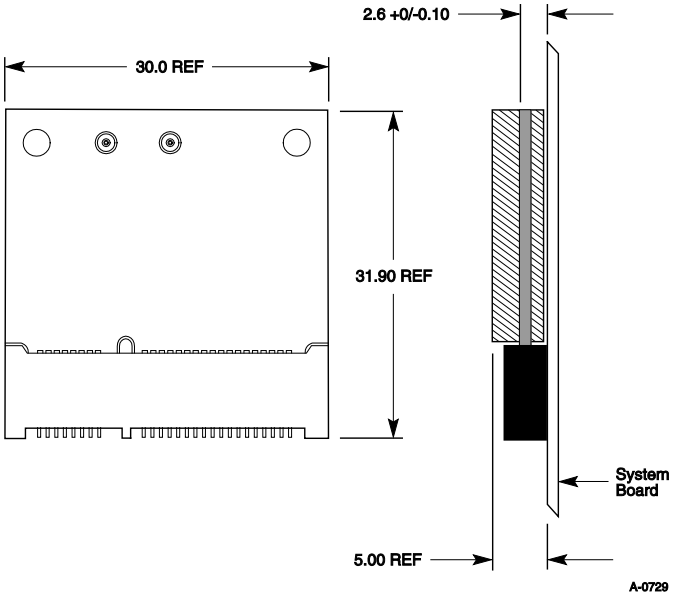


Figure 2-2: Half-Mini Card Form Factor (Wireless Example Application Shown)

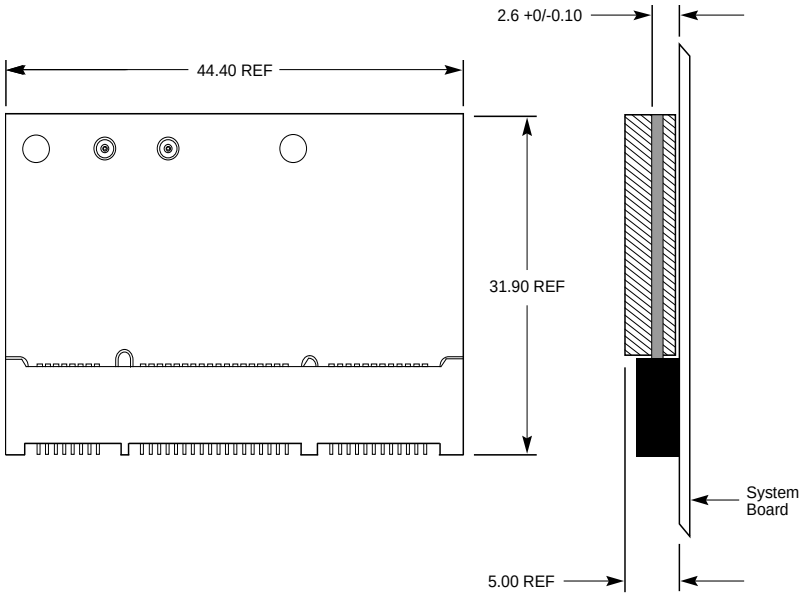


Figure 2-3: Display-Mini Card Form Factor (Wireless Example Application Shown)

2.2.2. Card and Socket Types

Given the multiple card sizes defined for Mini Card, host platforms have options with regard to socket configurations implemented to support each of the card sizes and potentially the mixing of the two card sizes within a common socket arrangement.

Single socket arrangements include those specific to Full-Mini Card (F1), Half-Mini Card (H1), and Display-Mini (D1) usages. These sockets specifically have the card retention features for only one size card and are further defined in Section 2.5.1.

Additionally, a single socket that optionally supports either a Full-Mini Card (F2) or a Half-Mini Card (H1 or H2) is possible to implement, this type being referred to as a dual-use socket and supports card retention for both size cards. See Section 2.5.2 for more details on this socket definition.

A dual head-to-head socket is defined as an optional way to incorporate two socket connectors (identified as A and B) into a space that most closely replaces a single Full-Mini socket. This arrangement offers the choice of installing two Half-Mini Cards (one of which ~~has to~~must be a H2 type) or one Full-Mini Card (F2) enabling some additional flexibility for a selection of BTO options. See Section 2.5.3 for more details on this socket definition.

Table 2-2 defines cross-compatibility for a series of defined card and socket types. It is important to notice that the dual head-to-head socket arrangement has special limitations ~~with regard to~~regarding card compatibility.

Table 2-2: Card and Socket Types Cross-Compatibility

Card Types		Full-Mini-Only Socket*	Half-Mini-Only Socket	Display-Mini Socket	Dual-Use Socket	Dual Head-to-Head Socket	
						Connector A	Connector B
F1	**Full-Mini***	Yes	No	No	No	No	No
F2	**Full-Mini with bottom-side keep outs**	Yes	No	No	Yes	Yes	No
H1	**Half-Mini**	No	Yes	Yes	Yes	Yes	No
H2	**Half-Mini with bottom-side keep outs**	No	Yes	Yes	Yes	Yes	Yes
D1	**Display-Mini**	No	No	Yes	No	No	No

* Equivalent to the original Mini Card defined card and socket in Revision 1.1 of this specification.

Mini Cards that were developed prior to this type definition are by default identified as Type F1. Given that the existing design meets the bottom-side keep out definition for Type F2, then subsequently identifying the product as Type F2 is acceptable.

2.2.3. Card PCB Details

The figures in this section provide the printed circuit board (PCB) details required to fabricate the card. The PCB for this application is expected to be 1.0 mm thick.

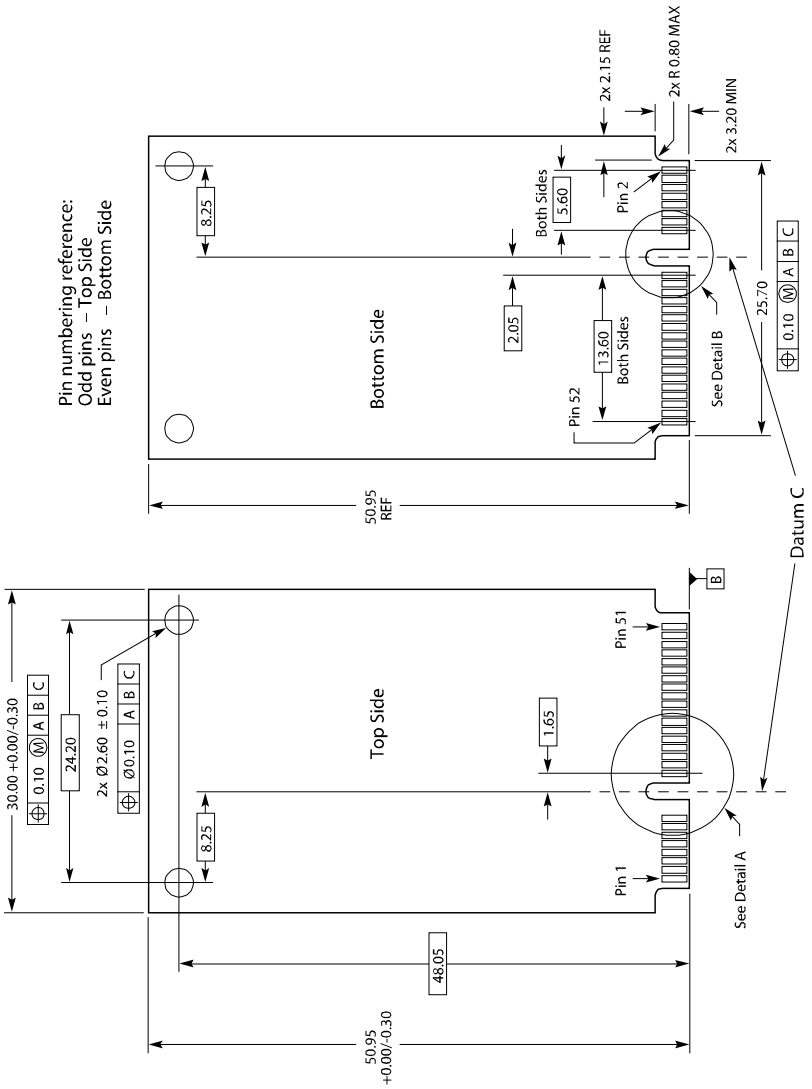


Figure 2-4: Full-Mini Card Top and Bottom

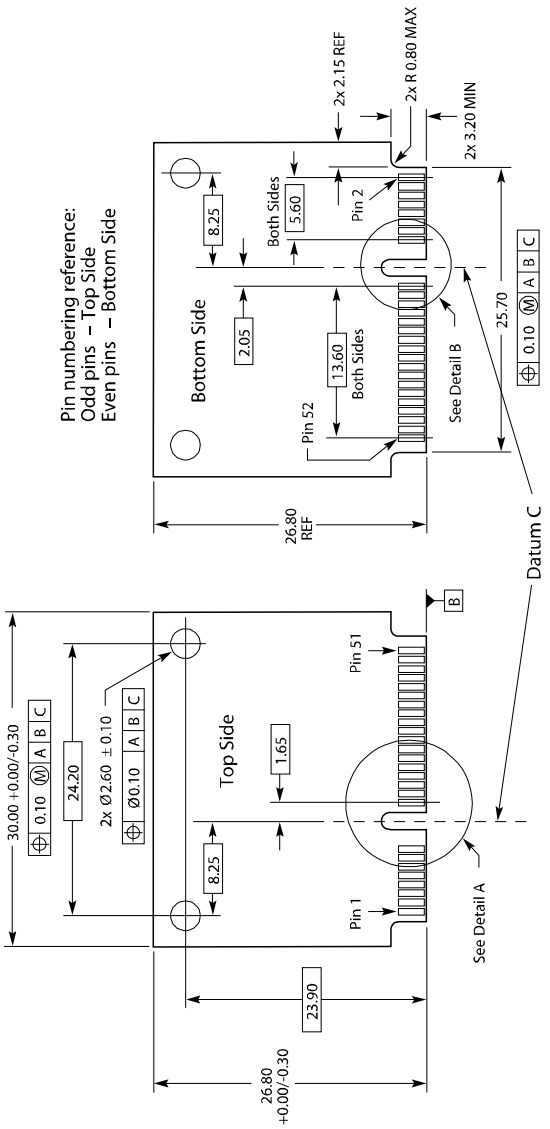


Figure 2-5: Half-Mini Card Top and Bottom

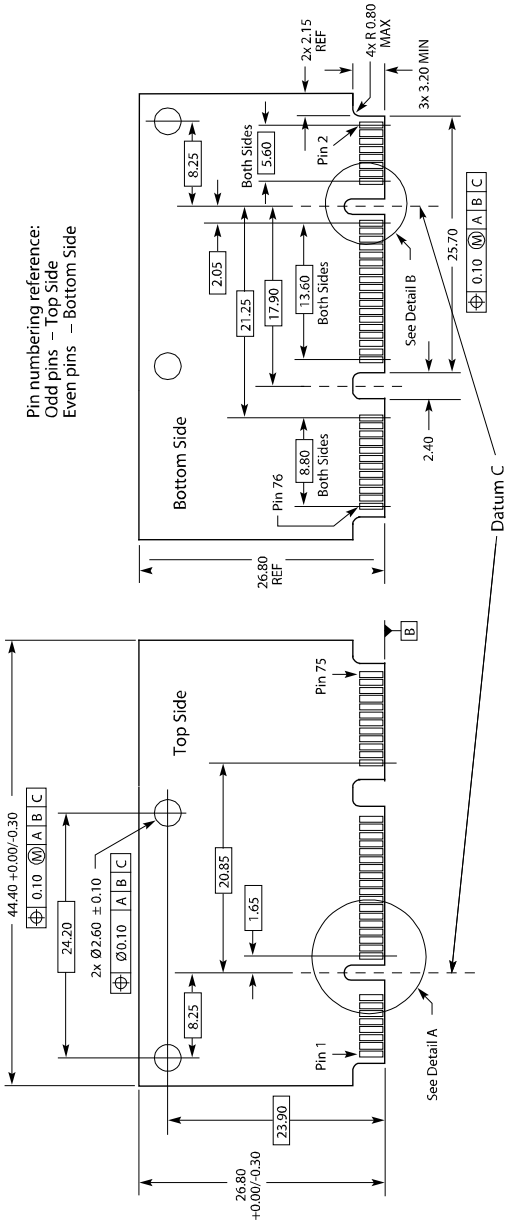


Figure 2-6: Display-Mini Card Top and Bottom

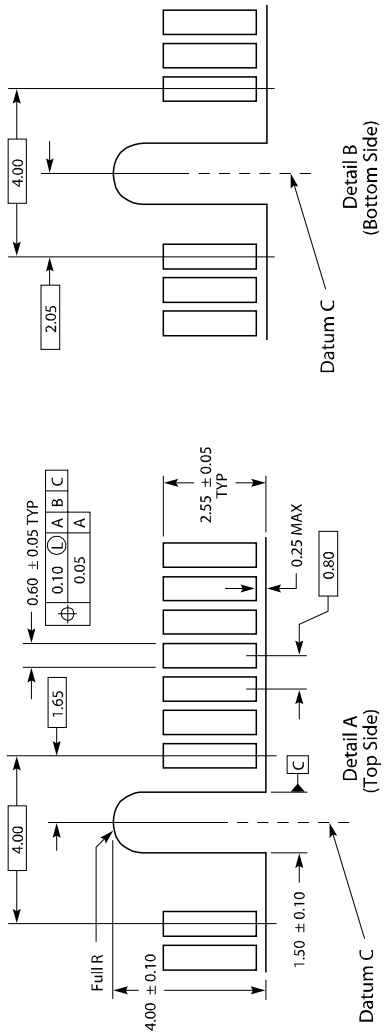


Figure 2-7: Card Top and Bottom Details A and B

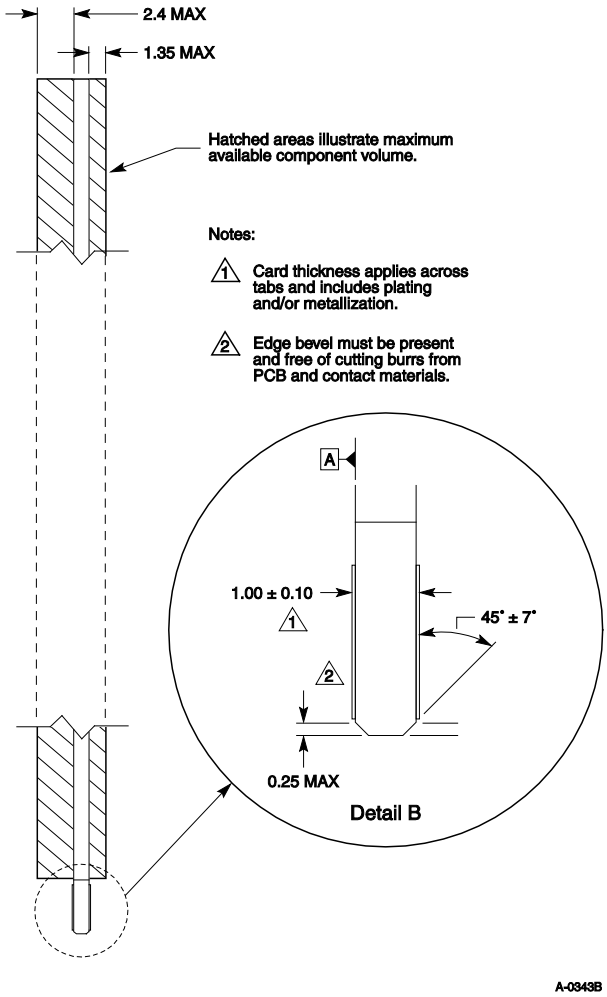


Figure 2-8: Card Edge

The remaining figures in this section provide details regarding the component keep out areas on Full-Mini (Types F1 and F2), Half-Mini Cards (Types H1 and H2), and Display-Mini Cards (D1).

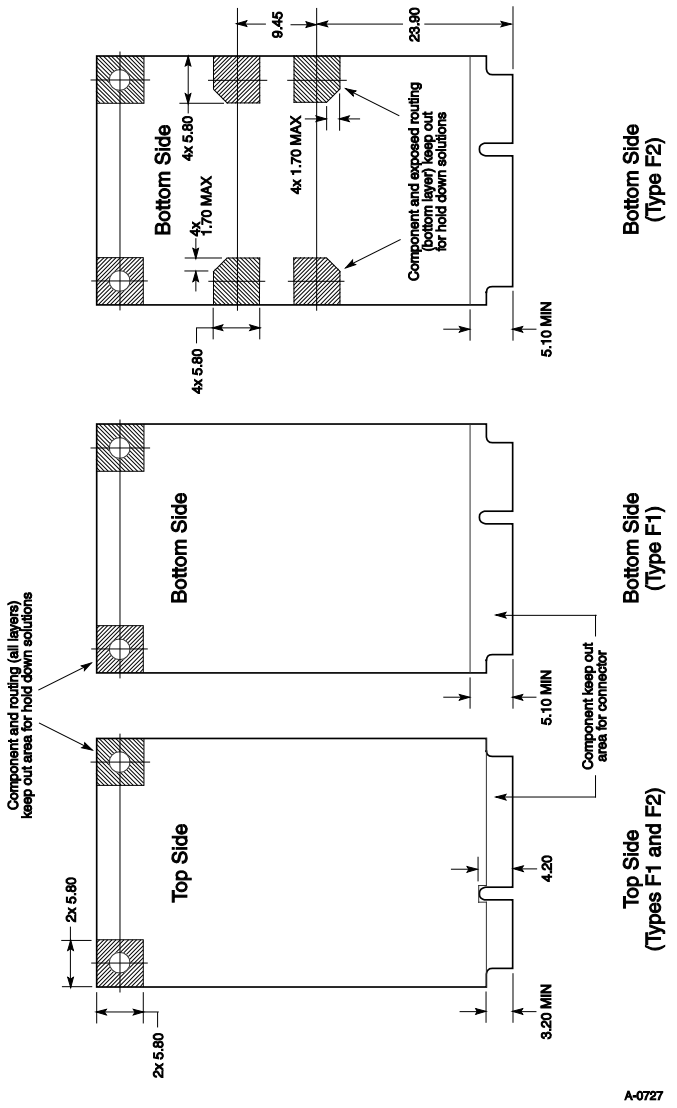


Figure 2-9: Card Component Keep Out Areas for Full-Mini Cards

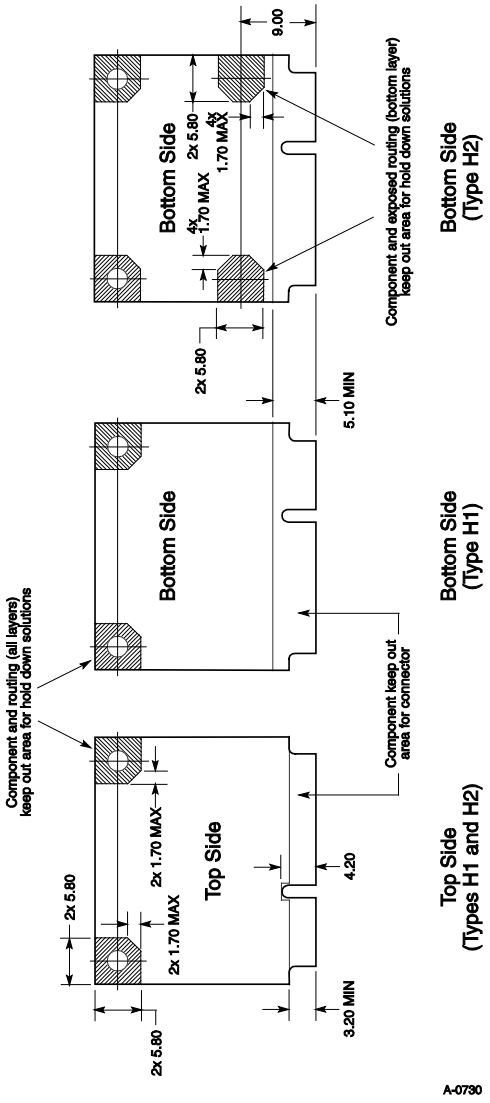


Figure 2-10: Card Component Keep Out Areas for Half-Mini Cards

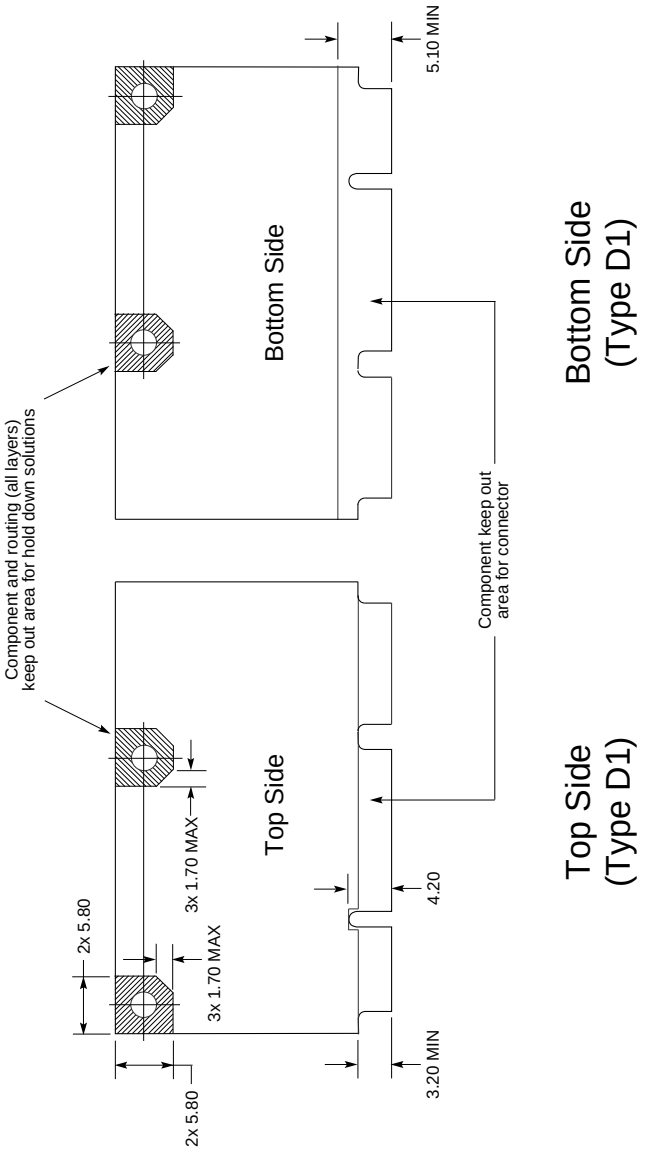


Figure 2-11: Card Component Keep Out Areas for Display-Mini Cards

2.3. System Connector Specifications

The PCI Express Mini Card system connector is ~~similar to~~like the SO-DIMM connector and is modeled after the Mini PCI Type III connector without side retaining clips.

Note: All dimensions are in millimeters, unless otherwise specified. All dimension tolerances are ± 0.15 mm, unless otherwise specified.

2.3.1. System Connector

The system connector for Full-Mini and Half-Mini is a 52-pin card edge type connector. Detailed dimensions should be obtained from the connector manufacturer. Figure 2-12 shows this version of the system connector.

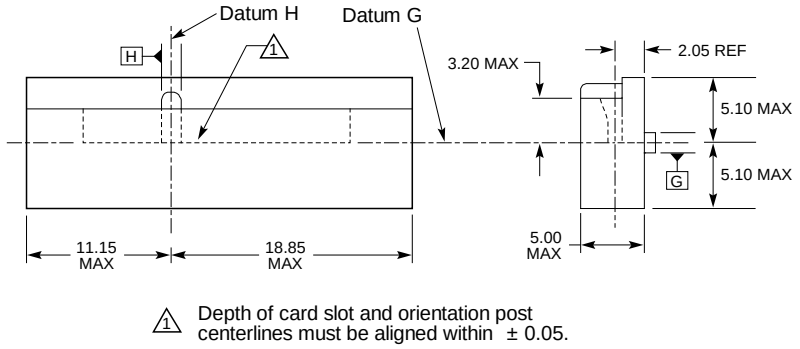


Figure 2-12: PCI Express Full-Mini and Half-Mini Card System Connector

The system connector for Display-Mini cards is a 76-pin card edge type connector. Detailed dimensions should be obtained from the connector manufacturer. Figure 2-13 shows this version of the system connector.

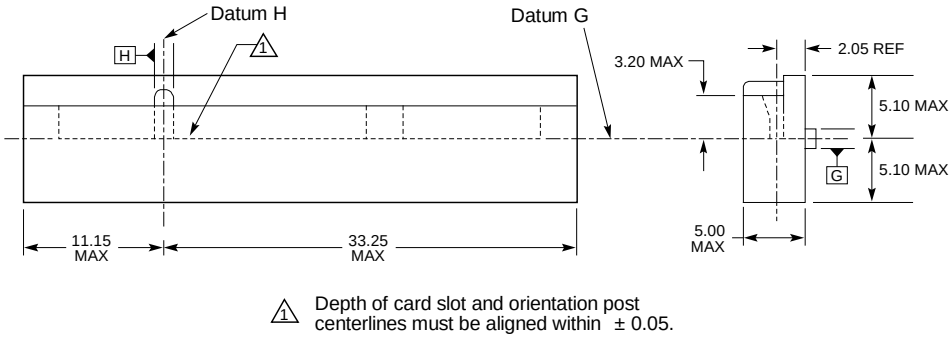


Figure 2-13: PCI Express Display-Mini Card System Connector

2.3.2. System Connector Parametric Specifications

The tables in this section specify the requirements for physical, mechanical, electrical, and environmental performance for the system connector.

Table 2-3: System Connector Physical Requirements

Parameter	Specification
Connector Housing	U.L. rated 94-V-1 (minimum) Must be compatible with lead-free soldering process
Contacts: Receptacle	Copper alloy
Contact Finish: Receptacle	Must be compatible with lead-free soldering process

Table 2-4: System Connector Mechanical Performance Requirements

Parameter	Specification
Durability	EIA-364-9 50 cycles
Total mating/unmating force*	EIA-364-13 2.3 kgf maximum
Shock	EIA-364-27, Test condition A Add to EIA-364-1000 test group 3 with LLCR before vibration sequence. Note: Shock specifications assume that an effective card retention feature is used.

* Card mating/unmating sequence:
1. Insert the card at the angle specified by the manufacturer.
2. Rotate the card into position.
3. Reverse the installation sequence to unmate.

Table 2-5: System Connector Electrical Performance Requirements

Parameter	Specification
Low Level Contact Resistance	EIA-364-23 55 mΩ maximum (initial) per contact; 20 mΩ maximum change allowed
Insulation Resistance	EIA-364-21 > 5 x 10^8 @ 500 V DC
Dielectric Withstanding Voltage	EIA-364-20 > 300 V AC (RMS) @ sea level
Current Rating	0.50 A/power contact (continuous) The temperature rise above ambient shall not exceed 30 °C. The ambient condition is still air at 25 °C. EIA-364-70 method 2
Voltage Rating	50 V AC per contact

Table 2-6: System Connector Environmental Performance Requirements

Parameter	Specification
Operating Temperature	-40 °C to +80 °C
Environmental Test Methodology	EIA-364-1000.01 Test Group, 1, 2, 3, and 4
Useful Field Life	5 years

To ensure that the environmental tests measure the stability of the connector, the add-in cards used shall have edge finger tabs with a minimum plating thickness of 30 micro-inches of gold over 50 micro-inches of nickel (for environmental test purposes only). Furthermore, it is highly desirable that testing gives an indication of the stability of the connector when add-in cards at the lower and upper limit of the card thickness requirement are used. In any case, both the edge tab plating thickness and the card thickness shall be recorded in the environmental test report.

2.4. I/O Connector Area

The placement of I/O connectors on a PCI Express Mini Card add-in card is recommended to be at the end opposite of the system connector and between the card hold down areas as shown in Figure 2-14~~Figure 2-14~~. The recommended area applies to both sides of the card, though typical placement will be on the top of the card due to the additional height available. Depending on the application, one or more connectors may be required to provide for cabled access between the card and media interfaces such as LAN and modem line interfaces and/or RF antennas. This area is not restricted to I/O connectors only and can be used for circuitry if not needed for connectors.

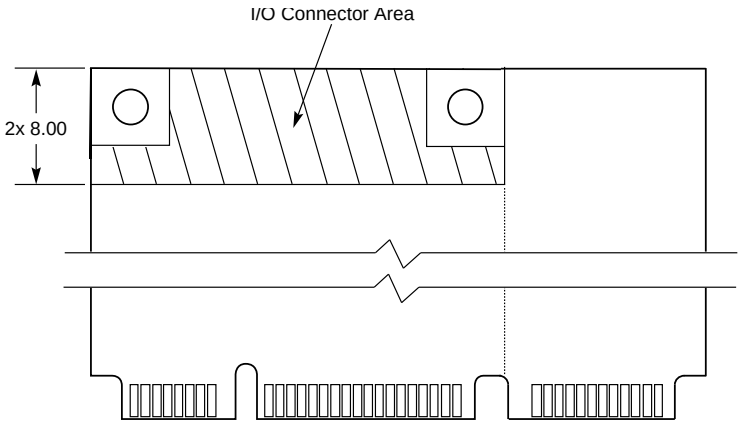


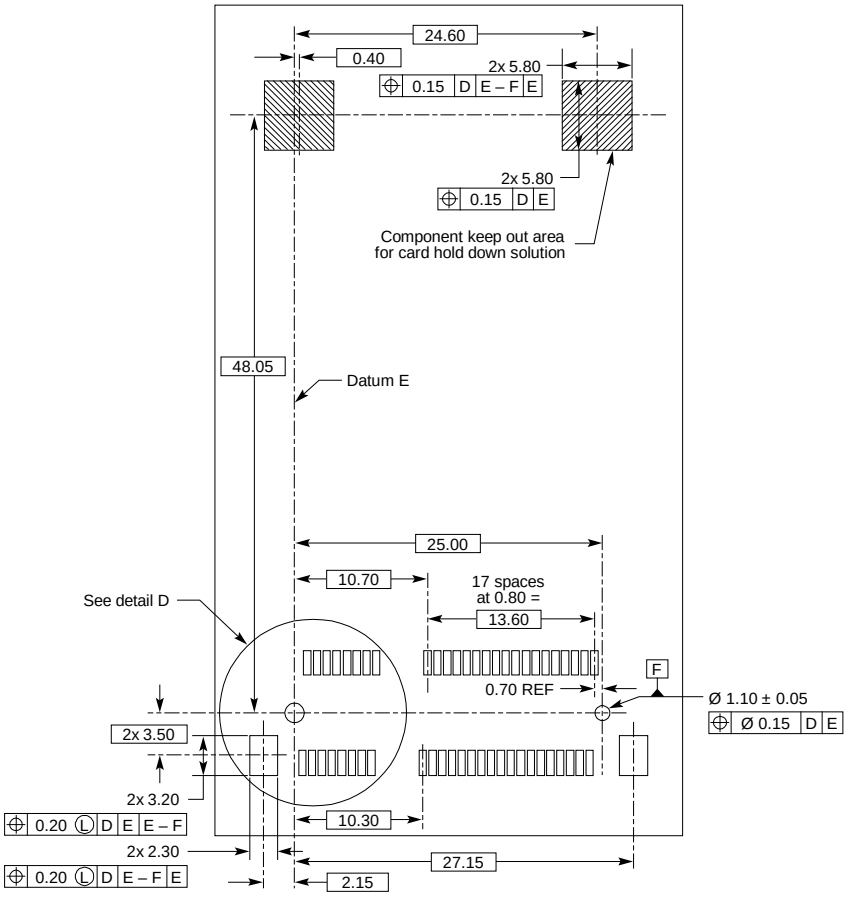
Figure 2-14: I/O Connector Location Areas

2.5. Recommended Socket Configurations

The following subsections address various recommended footprints for the system connector covering single-use sockets, dual-use sockets, and multi-socket configurations.

2.5.1. Single-Use Full-Mini and Half-Mini Sockets

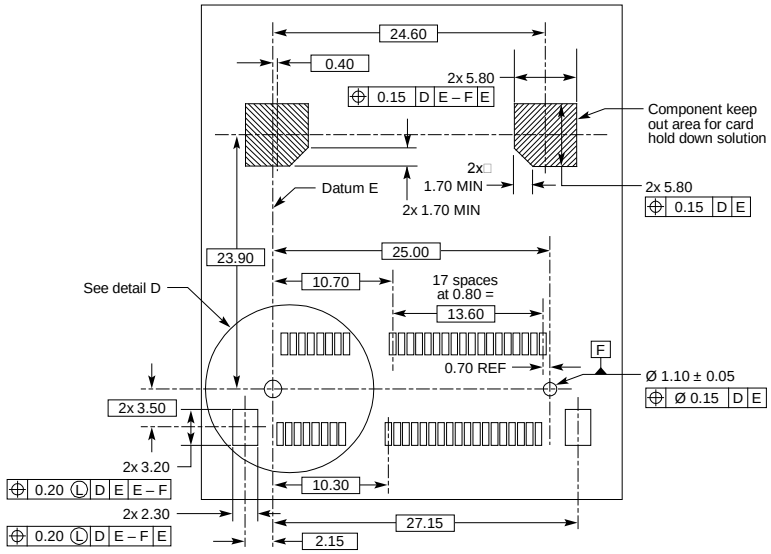
The figures in this section show the recommended system board layouts for single-use sockets specific to Full and Half-Mini Card applications. As a Display-Mini Card socket supports dual-use with Half-Mini Card, its definition is covered in Section 2.5.2.



Notes:

1 Datum D is the top surface of PCB.

Figure 2-15: Recommended System Board Layout for Full-Mini-Only Socket



Notes:

1 Datum D is the top surface of PCB.

Figure 2-16: Recommended System Board Layout for Half-Mini-Only Socket

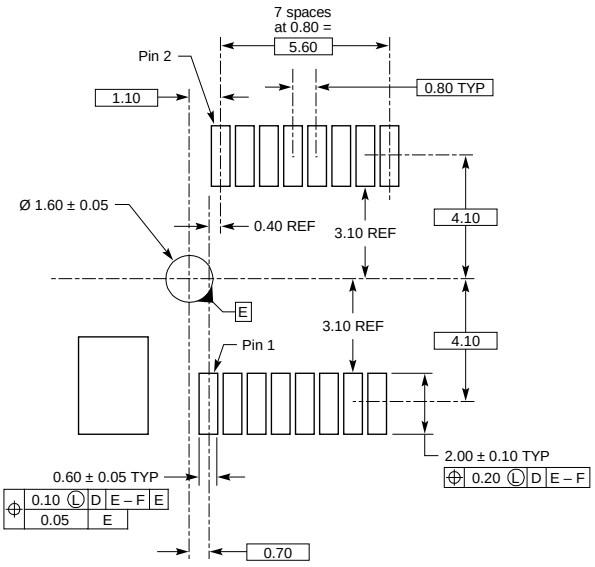


Figure 2-17: Recommended System Board Layout (Detail D)

2.5.2. Dual-Use Sockets

This section defines two dual-use sockets: a dual-use Full/Half-Mini Card socket and a dual-use Display/Half-Mini Card socket.

Figure 2-18 illustrates the concept of a dual-use socket that can accept either a Full-Mini Card or a Half-Mini Card. This socket differs from the Full-Mini-only socket in that consideration is given to support hold down support for the installation of a Half-Mini Card into the same socket. All Full and Half-Mini Cards, ~~with the exception of~~except for the Type F1 Full-Mini Card, are compatible with this socket.

Figure 2-19 shows the recommended system board layout for the Full/Half-Mini Card dual-use socket.

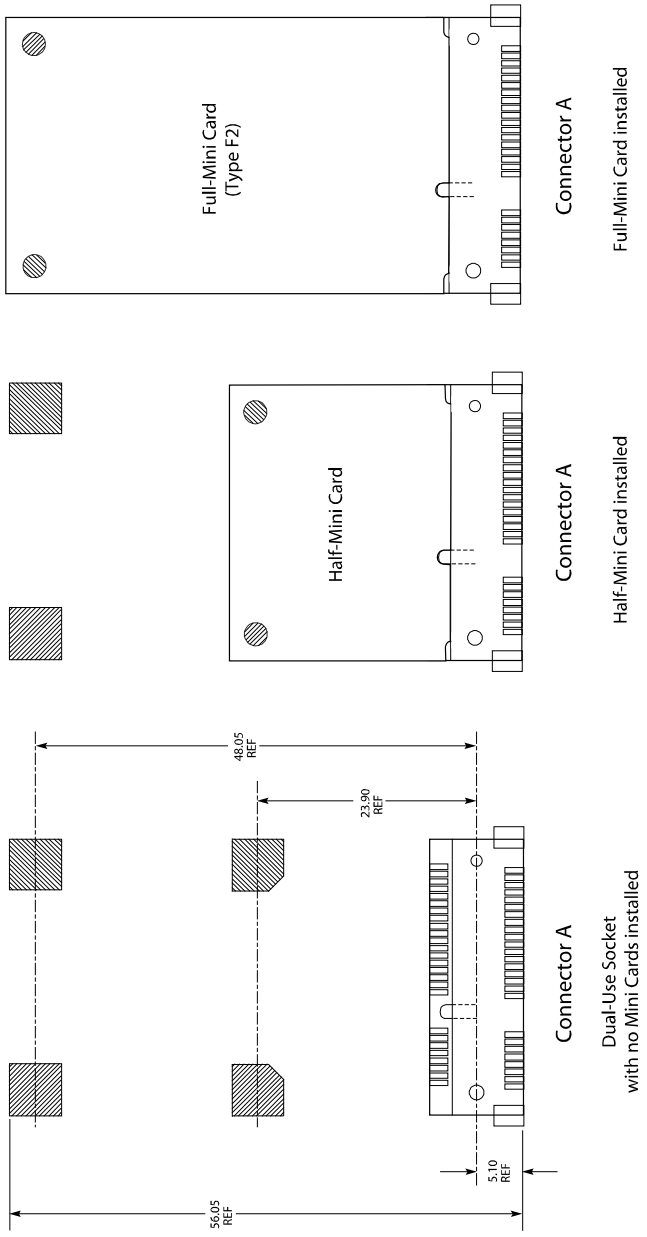
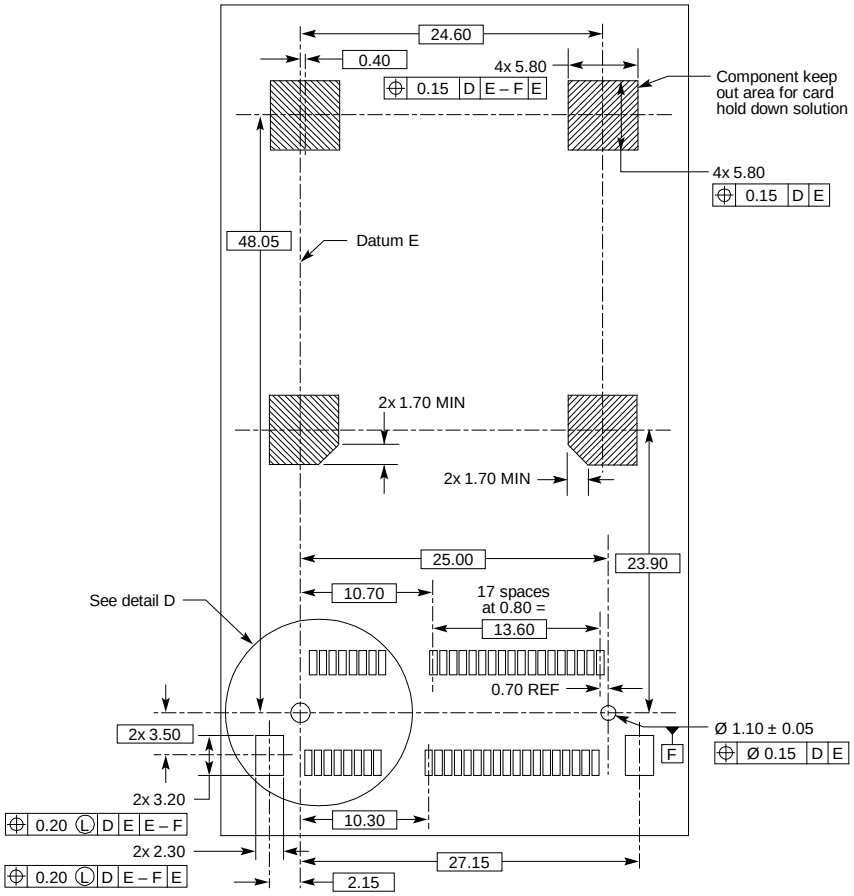


Figure 2-18: Dual-Use Socket

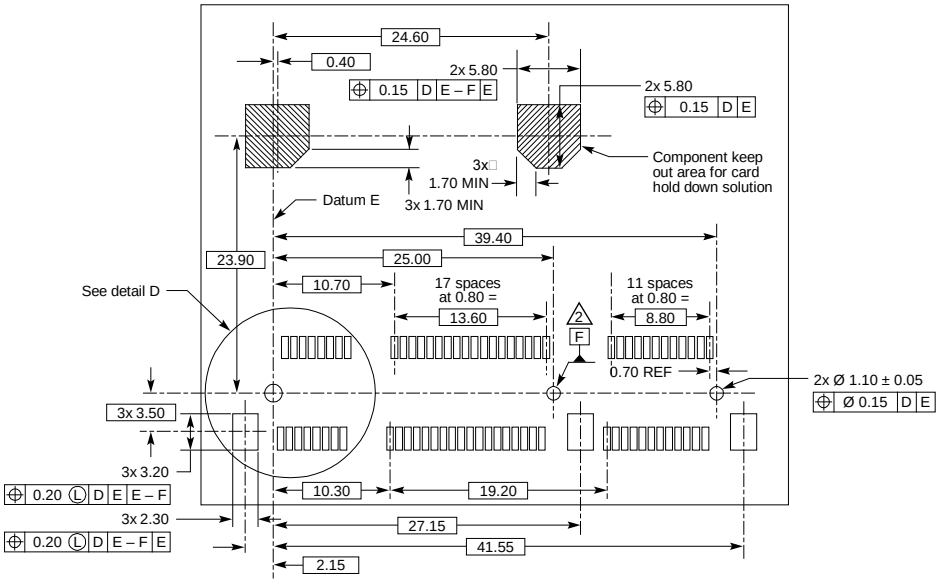


Notes:

1 Datum D is the top surface of PCB.

Figure 2-19: Recommended System Board Layout for Dual-Use Full/Half-Mini Card Socket

Figure 2-20 shows the recommended system board layout for a dual-use socket that can accept either a Display-Mini Card or a Half-Mini Card. While this socket uses the 76-pin system connector specific to the Display-Mini Card application, the hold down support allows for the installation of a Half-Mini Card into the same socket. All Display-Mini and Half-Mini Cards are compatible with this socket.



Notes:

1 Datum D is the top surface of PCB.

2 This hole is optional and is only needed if a single footprint on an assembly is to be used to mount either the 52 pin or 76 pin connector.

Figure 2-20: Recommended System Board Layout for Dual-Use Display/Half-Mini Card Socket

2.5.3. Dual Head-to-Head Sockets

Figure 2-21 illustrates the concept of a dual head-to-head socket configuration. This optional configuration defines a two connector (A and B) solution that is intended to allow installation for either one Full-Mini Card or two Half-Mini Cards. Figure 2-22 shows the recommended system board layout for this configuration based on overlaying the defined dual-use and Half-Mini-only sockets (see Figure 2-16 and Figure 2-19 for additional dimensional details).

It is important to note the limitations regarding card compatibility with this socket configuration. Connector A can accept all but the Type F1 Full-Mini Card. Connector B can only accept Type H2 Half-Mini Cards. When using two Half-Mini Cards in this configuration, care must be taken that at least one of those cards be Type H2.

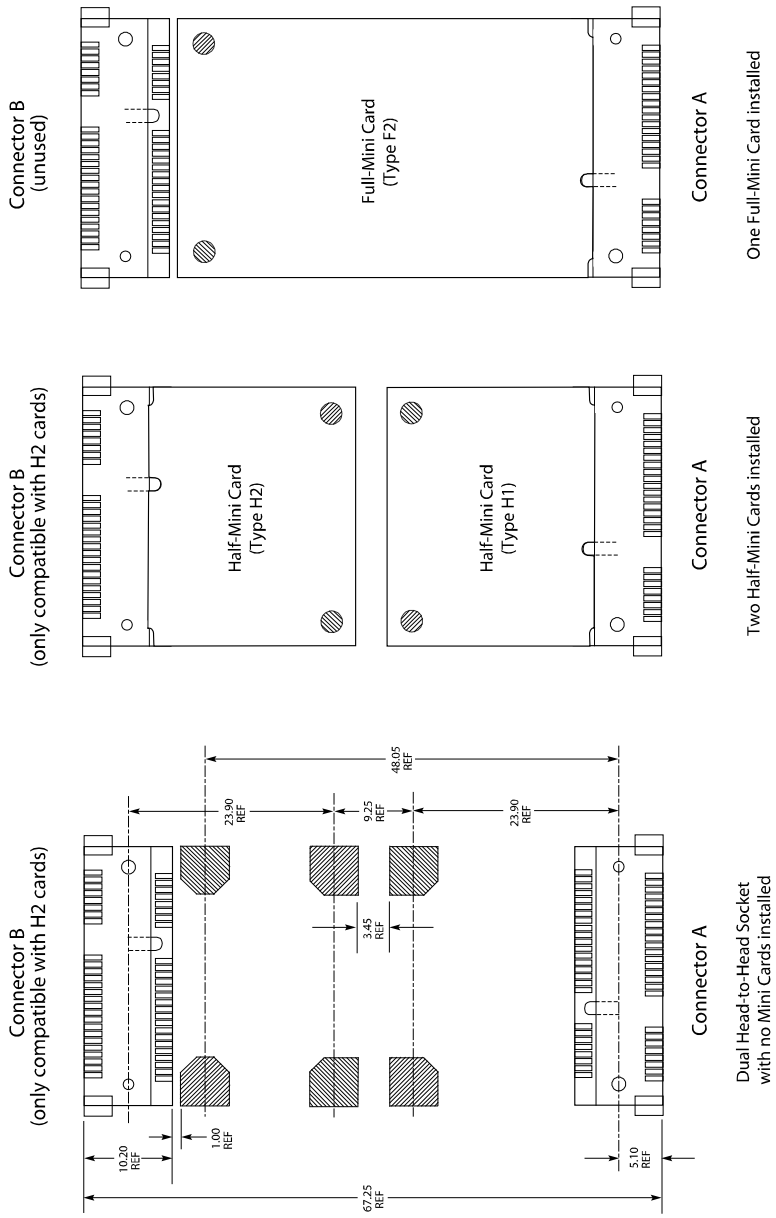
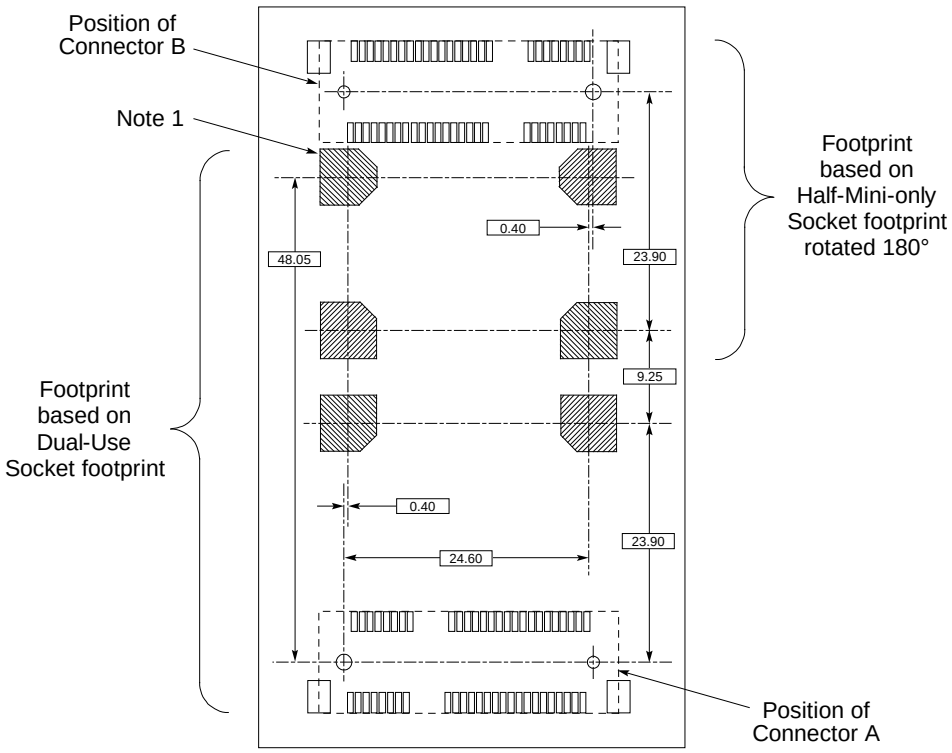


Figure 2-21: Dual Head-to-Head Socket



Notes:

1 The two keepout areas at the top of the Dual-Use Socket footprint vary in this layout to match those defined for the bottom side only keepouts for the Half-Mini Type H2.

2 Refer to Figure 2-16 for feature dimensions, tolerances and control frames.

Figure 2-22: Recommended System Board Layout for Dual Head-to-Head Sockets

2.5.4. Side-by-Side Socket Spacing

Figure 2-23 shows the recommendation for placing Full and Half-Mini Card sockets side-by-side on a system board. This recommendation can be combined with any of the other system board recommendations for increased flexibility in managing multiple cards in a single platform.

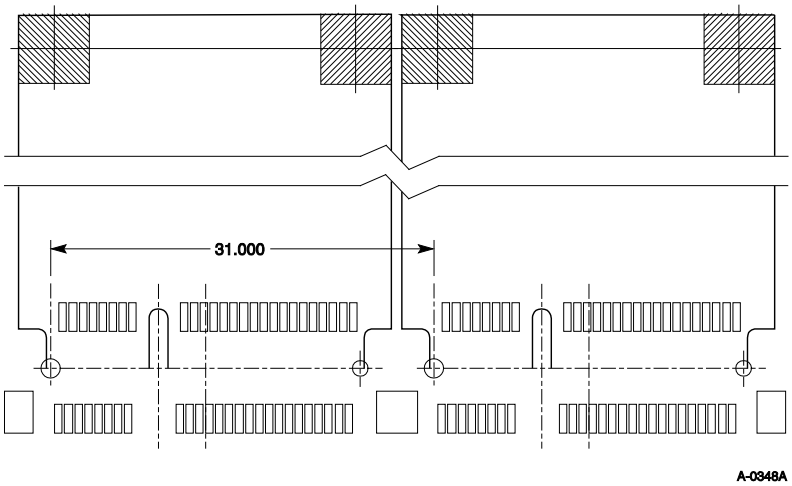


Figure 2-23: Recommended System Board Layout (Full and Half-Mini Card Side-by-Side Spacing)

2.6. Thermal Guidelines

The following thermal guidelines are intended to provide guidance to both system board designers and PCI Express Mini Card add-in card designers.

2.6.1. Thermal Design Definitions

The *Thermal Design Power* (TDP) is the steady state electrical power that is converted to heat and dissipated by a card or any heat source. The TDP is less than the electrical power and as an example could be the electrical power minus the radiated power in a wireless radio.

Steady state is defined as the operational application profile that represents the normal use scenario for the product being specified. This might include a series of radio transmissions and receptions occurring at a regular interval that is representative of actual use within normal bounds for the network being used. A maximum TDP would be based on a steady state condition associated with the scenario that dissipates the maximum average power.

A *thermal guideline* is a non-normative technical discussion or objective that could be used to describe the design or the conditions in which it operates.

In cases where either the system board or PCI Express Mini Card add-in card does not strictly follow the guidelines, a coordinated solution between the card and the host platform vendor is dictated. Solutions might be able to manage higher thermals by implementing features that may include passive (e.g., thermal insulation, thermal spreading) and active (e.g., thermal-based throttling) techniques. Such techniques are not comprehended by this specification.

2.6.2. Thermal Guidelines for PCI Express Mini Card Add-in Card Designers

This section provides guidelines for PCI Express Mini Card add-in card designers to follow to assure compatibility with host systems.

For purposes of this specification, power consumption is not necessarily directly related to the thermal dissipation limitations within the system; e.g., additional power may be consumed via the system interface, yet the thermal energy may be dissipated in circuits located off the card (most likely in a remote media interface circuit such as an antenna). Power consumption limits for PCI Express Mini Card are included in Chapter 3.

System Board Requirements:

- System board designers shall ensure that the board can dissipate 28.1 °C/W in the region of the add-in card. The method in which this is dissipated depends on the OEM standards, but natural convection/radiation is unlikely. Most applications will require some air flow over the add-in card.
- Direct attach thermal solutions are not allowed.

Add-In Card Requirements:

- The maximum thermal dissipation directly from any PCI Express Full and Half Mini Card add-in card is 2.3 W at a component temperature of 90 °C and 65 °C ambient temperature inside the host and around the add-in card.
- The maximum thermal dissipation directly from any PCI Express Display-Mini Card add-in card is 3.3 W at a component temperature of 90 °C and 65 °C ambient temperature inside the host and around the add-in card.
- De-rate maximum card power 0.046 W for every 1 °C component T_{CASE} is rated below 90 °C.
- Example: T_{CASE} = 85 °C, then de-rate power 0.23 W to P = 2.07 W.
- The total thermal energy dissipated must be spread out relatively uniformly over the PCI Express Mini Card add-in card in order to avoid hot spots. Figure 2-24~~Figure 2-24~~ provides guidance on power density. The top side of the card can generally tolerate as much as twice the density as the bottom side of the card, with the components on the bottom side being trapped between the add-in card PCB and the system board PCB.

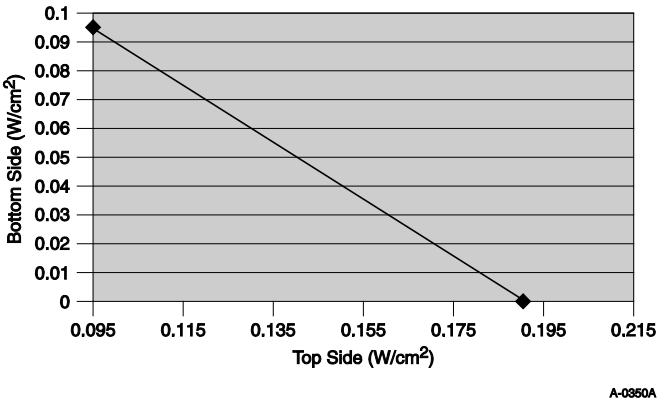


Figure 2-24: Power Density Uniform Loading at 80 Percent Coverage

Example: If side one of the card is loaded to 0.12 W/cm^2, the other side of the card (side two) can only be loaded to 0.07 W/cm^2. In all cases, the sum of power densities for both sides of the card should not exceed 0.19 W/cm^2.

Note: Additional heat beyond the maximum 2.3 W of thermal dissipation, listed on page 37 as a requirement for an add-in card, may be generated by the PCI Express Mini Card add-in card's I/O circuitry. For example, for certain modem line conditions in the approved countries, TBR21 states a modem may dissipate as much as an additional 2.4 W (40-V drop at 60 mA). If the add-in card requires additional thermal management ~~in order~~ to stay within the aforementioned criteria, the add-in card manufacturer must coordinate with the system board manufacturer to achieve a final solution.

2.6.2.1. Implementation Considerations

The following points should be considered when developing a PCI Express Mini Card add-in card's thermal design.

- It is accepted that some host platform designs may be designed to support higher TDP limits and, if so, this should be noted by the vendor as a capability beyond the basic assumptions made in establishing the guidelines in this specification.
- The component temperature of 90 °C is an ergonomic requirement so that the customer is not discomforted by the temperature of the PCI Express Mini Card add-in card when using the computer. The 90 °C component temperature is meant to assure that no greater than a 65 °C skin temperature is experienced when touching the exterior of the host device. UL 60950-1 temperature limits could also be considered.
- The card's TDP should be spread out relatively uniformly over the assembly. Higher TDP components should not be co-located.
- The host platform encloses the card thermally with no forced convection and no predictable or well-defined natural convection air buoyancy path.

- Thermal impact of card materials should be considered for temperature rise and for allowable touch temperature.
- The card PCB may need thermal vias to help conduction and heat spreading for high TDP components.
- The maximum ambient rating for the card may be determined by measuring the card surface temperature when installed in the host unpowered.

2.6.3. Thermal Guidelines for Integrating Wireless Wide Area Network Mini Card Add-in Cards

This section provides guidelines for host system board designers to follow to assure compatibility with Wireless Wide Area Network (WWAN) PCI Express Mini Card add-in cards.

It is recommended that system board designers meet the following requirements:

- For WWAN add-in cards, Thermal Dissipation = Electrical Input Power – Antenna Output Power. For WWAN, thermal dissipation can be inferred by measuring electrical input power and antenna output power. Another technique is to add up the maximum thermal dissipation from all components from specification sheets or through measurements.
- Design for the maximum TDP based upon the technology. The worst case WWAN add-in card can dissipate up to 3.1 W of thermal energy as shown in Table 2-7.

Table 2-7: Maximum TDP

WWAN Technology	Maximum TDP
W-CDMA HSDPA 1900 @ 22 dBm	2.9 W – 3.1 W
W-CDMA HSDPA 850 @ 22 dBm	2.8 W – 3.0 W
W-CDMA HSDPA 2100 @ 22 dBm	2.7 W – 2.7 W
CDMA 2000 1xEVDO @ 24 dBm	2.7 W – 2.9 W
GPRS Class 10 @ 32 dBm	1.8 W

- Design to a maximum component surface temperature of 85 °C. Components in a WWAN add-in card typically have a maximum surface temperature of 85 °C.
- WWAN add-in cards must operate within their product specification. Power amplifiers are the main heat generators.

  Temperature delta from host to WWAN device at reference PCB area:

  - 0 °C – 20 °C (WWAN idle)
  - 20 °C – 40 °C (WWAN active, still air)

  Temperature delta between PA and reference PCB area:

  - 20 °C – 30 °C (WWAN active)

- The WWAN add-in card temperature profile depends on host cooling approach including:
  - Natural convection
  - Forced air
  - Direct attach
- Location of "heat sources" near the WWAN add-in card can negatively impact the thermal design. Do not place the add-in card near other host heat sources or "down wind" from such heat sources.
  - Host CPU's and graphics cards are both heat (and noise) sources.
- Inadequate cooling may cause the WWAN add-in card to overheat:
  - WWAN devices monitor internal temperature to ensure RF performance will be met over target temperature range.
  - Required for FCC compliance on Transmitter.
  - Overheated modules may have shortened lifespan (field returns).
- To be conservative, the thermal design of the system board must consider the TDP of the worst-case operating mode of the WWAN add-in card. The worst case mode is when a WWAN add-in card is sitting on the edge of a cell and continuously transmitting data. For example, this may occur if a camera is attached to the host.
- The WWAN add-in card typically does not operate in the worst-case operating mode. For example, consider CDMA 2000 1xEVDO. The Maximum Thermal Dissipation varies based upon the distance from the base station:
  - Maximum Thermal Dissipation = 1.0 W (close to the base station)
  - Maximum Thermal Dissipation = 1.8 W (middle of the cell)
  - Maximum Thermal Dissipation = 2.7 W (edge of the cell)

  These values are representative. Maximum input voltage is assumed.

  The CDMA 2000 1xEVDO network is constantly sending power control bits to the WWAN add-in card to control the output power. CDMA requires devices to transmit power at the lowest possible level to provide reliable service across the cell.

  CDMA 2000 1xEVDO devices go into a power save mode called dormancy on their own after at least 20 seconds of data inactivity.

  Dormant state:
  - Average Thermal Dissipation: << 1 W
  - Maximum Thermal Dissipation: < 1 W
- The Average Thermal Dissipation is function of the user-level application that is running and the distance from the base station. Most business applications enable the device to go dormant thereby lowering the average thermal dissipation.
  - Average Thermal Dissipation < Maximum Thermal Dissipation

- Applications that perform data streaming such as VOIP, video streaming from an attached camera or streaming audio prevent the device from going dormant.
  - Average Thermal Dissipation = Max Thermal Dissipation
- The host should support the USB Selective Suspend feature to reduce electrical power consumption and thermal dissipation by the WWAN add-in card.
- System board designers must consider WWAN in their platform thermal design from the beginning. It is difficult to retrofit WWAN in existing platforms.

3

3. Electrical Specifications

3.1. Overview

This chapter covers the electrical specifications for PCI Express Mini Card.

3.2. System Interface Signals

Table 3-1 summarizes the 26 signal and 18 power lines that are supported by the system interface.

Table 3-2

~~Table 3-2~~ summarizes the additional 13 signals needed to support Display-Mini Card in the system interface.

Three primary data interfaces are defined for PCI Express Mini Card: PCI Express, USB, and DisplayPort. System designers may optionally choose to implement slots that support only a subset of these interfaces and still be compliant to this specification. As PCI Express Mini Card is targeted to BTO/CTO applications, the proper matching of specific add-in cards to systems with the matching data interface has to be managed by the system integrator.

Table 3-1: PCI Express Mini Card System Interface Signals

Signal Group	Signal	Direction	Description
Power	+3.3Vaux (5 pins)		3.3 V source
	+1.5V (3 pins)		1.5 V source
	GND (14 pins)		Return current path
PCI Express	PETp0, PETn0 PERp0, PERn0	Input/Output	PCI Express x1 data interface: one differential transmit pair and one differential receive pair
	REFCLK+, REFCLK–	Input	PCI Express differential reference clock (100 MHz)
Universal Serial Bus (USB)	SSTX+ SSTX- SSRX+ SSRX-	Input/Output	~~USB 3.0~~USB3.1 Gen1 SuperSpeed serial data interface. One differential transmit pair and one differential receive pair (Note: these signals overlay the PCI Express x1 data interface at the socket)
	USB_D+, USB_D–	Input/Output	USB serial data interface compliant to the USB 2.0 specification

Signal Group	Signal	Direction	Description
Auxiliary Signals (3.3V Compliant)	PERST#	Input	Functional reset to the card
	CLKREQ#	Input/Output	Reference clock request signal. Also used by L1 PM Substates
	WAKE#	Input/Output	Open Drain active Low signal. When the add-in card supports wakeup, this signal is used by the add-in card to request that the system return from a sleep/suspended state to service a function initiated wake event. When the add-in card supports the OBFF mechanism, this signal is used by the system to indicate OBFF or CPU Active State transitions.
	SMB_DATA	Input/Output	SMBus data signal compliant to the SMBus 2.0 specification
	SMB_CLK	Input	SMBus clock signal compliant to the SMBus 2.0 specification
Communications Specific Signals	LED_WPAN#, LED_WLAN#, LED_WWAN#	Output	Open drain, active low signals. These signals are used to allow the PCI Express Mini Card add-in card to provide status indicators via LED devices that will be provided by the system.
	W_DISABLE1#, W_DISABLE2#	Input	Active low signals. These signals are used by the system to disable radio operation on add-in cards that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the card.
User Identity Module (UIM) Signals	UIM_PWR (1 pin)	Output	Power source for the UIM. Compliant to the ISO/IEC 7816-3 specification (VCC).
	UIM_RESET	Output	UIM reset signal. Compliant to the ISO/IEC 7816-3 specification (RST).
	UIM_CLK	Output	UIM clock signal. Compliant to the ISO/IEC 7816-3 specification (CLK).
	UIM_SPU	Input/Output	Standard or proprietary use signal. Compliant to the ISO/IEC 7816-3 specification (SPU).

Commented [TS1]: ECN_L1_PM_Substates_with_CLKREQ_31_May_2013_Rev10a

Signal Group	Signal	Direction	Description
	UIM_DATA	Input/Output	UIM data signal. Compliant to the ISO/IEC 7816-3 specification (I/O).
	UIM_IC_DP	Input/Output	Inter-Chip USB D+ Data line
	UIM_IC_DM	Input/Output	Inter-Chip USB D- Data line

Table 3-2: PCI Express Display-Mini Card System Interface Signals

Signal Group	Signal	Direction	Description
DisplayPort	ML0p, ML0n ML1p, ML1n ML2p, ML2n ML3p, ML3n	Input or Output	DisplayPort main link data interface: four unidirectional differential pairs, signal direction dictated by MLDIR
	AUXp, AUXn	Input or Output	DisplayPort auxiliary channel, signal direction dictated by MLDIR
	HPD	Input or Output	Hot Plug Detect, signal direction dictated by MLDIR
	MLDIR	Input/Output	DisplayPort data interface direction
	DMC#	Output	Display-Mini Card present

3.2.1. Power Sources and Grounds

PCI Express Mini Card provides two power sources: one at 3.3Vaux (3.3Vaux) and one at 1.5V (+1.5V). The auxiliary voltage source, +3.3Vaux, may be the only supply voltage available during the system's stand-by/suspend state to support wake event processing on the communications card. The 1.5V voltage source may or may not be present in the low power state. The 1.5-V power source is sharing functionality with a coexistence pin and tunable antenna pins, see ~~s~~Sections 3.3.2 ~~3.3.2~~ and 3.3.4~~3.3.3~~. Whether the add-in card is using any of these pins for coexistence support, tunable antenna control or a 1.5V power source is OEM-specific and shall be documented by the OEM.

Commented [TS2]: Per Combined Antenna Tuning/Coexistence Signal ECN

3.2.2. PCI Express Interface

The PCI Express interface supports a x1 PCI Express interface (one Lane). A Lane consists of an input and an output high-speed differential pair. Also supported is a PCI Express reference clock. Refer to the *PCI Express Base Specification* for more details on the functional requirements for the PCI Express interface signals.

The PCI Express interface and the ~~USB 3.0~~USB3.1 Gen1 interface cannot operate simultaneously, ~~because~~ as they share the same pins. How the platform selects which of the two interfaces to activate is platform-specific.

IMPLEMENTATION NOTE

Lane Polarity

By default, the PETp0 and PETn0 pins (the transmitter differential pair of the connector) shall be connected to the PCI Express transmitter differential pair on the system board and to the PCI Express receiver differential pair on the PCI Express Mini Card add-in card. ~~Similarly~~Similarly, by default, the PERp0 and PERn0 pins (the receiver differential pair of the connector) shall be connected to the PCI Express receiver differential pair on the system board and to the PCI Express transmitter differential pair on the PCI Express Mini Card add-in card.

However, the "p" and "n" connections may be reversed to simplify PCB trace routing and minimize vias if needed. All PCI Express receivers incorporate automatic Lane polarity inversion as part of the Link initialization and training and will correct the polarity independently on each Lane. Refer to Section 4.2.4 of the *PCI Express Base Specification* for more information on Link initialization and training.

IMPLEMENTATION NOTE

Link Power Management

PCI Express Mini Card add-in cards that implement PCI Express-based applications are required by the *PCI Express Base Specification* to implement Link power management states, including support for the L0s and L1 (in addition to the primary L0 and L3 states). For PCI Express Mini Card implementations, Active State PM for both L0s and L1 states shall also be enabled by default. Refer to Section 5.4 of the *PCI Express Base Specification* for more information regarding Active State PM.

3.2.3. USB Interface

The USB 2.0 interface supports USB 2.0 in all three modes (Low Speed, Full Speed, and High Speed). Since there is not a separate USB-controlled voltage bus, USB functions implemented on a PCI Express Mini Card add-in card are expected to report as self-powered devices. All electrical characteristics, enumeration, bus protocol, and bus management features for this interface are defined by ~~*Universal Serial Bus*~~*USB 2.0 Specification*~~*, Revision 2.0*~~.

USB-based Mini Cards that implement a wakeup process are required to use the in-band wakeup protocol as defined in the *Universal Serial Bus Specification* and shall not use the WAKE# signal to enable the in-band wakeup process.

The USB3.1 interface supported is USB3.1 Gen1, 5 Gbps (refer to the *USB3.1 Specification*).~~The USB 3.0 interface supports USB 3.0 (Superspeed) at Gen 1.~~ The SuperSpeed differential transmit lines (SSTX+, SSTX-) are required to implement the transmit path of a ~~USB 3.0~~USB3.1 Gen1 SuperSpeed interface. These pins shall be connected to the transmitter differential pair in the system and to the receiver differential pair on the module.

Likewise, SuperSpeed differential receive lines (SSRX+, SSRX-) are required to implement the receive path of a ~~USB 3.0~~USB3.1 Gen1 SuperSpeed interface. These pins shall be connected to the receiver differential pair in the system and to the transmitter differential pair on the module.

For host systems that implement ~~USB 3.0~~USB3.1 Gen1 support, the SuperSpeed differential transmit/receive pins are shared with the PCI Express interface.

The ~~*Universal Serial Bus*~~*USB 3.1 Specification*~~,~~ ~~Revision 3.0~~ defines all electrical characteristics, enumeration, bus protocol and bus management features for this interface. If the ~~USB 3.0~~USB3.1 Gen1 interface is not supported, then the four SuperSpeed differential pins may be used as PCI Express differential pins.

3.2.4. DisplayPort Interface

The DisplayPort interface supports a full-featured implementation as defined in the referenced *DisplayPort Specification*. A full four lane implementation of the main link, the auxiliary channel, and hot plug detect (HPD) is supported. Additionally, two system level signals, DMC# and MLDIR, are provided to assist in configuration of the platform when a Display-Mini Card is installed.

3.2.4.1. HPD

The HPD signal connects to the standard Hot Plug Detect signal of the DisplayPort interface. The intent of this signal is to indicate to the DisplayPort source that an active display is connected. The logical direction of HPD is determined by the state of MLDIR.

For a wireless display application, HPD being asserted shall also be an indication that the wireless link between the system and the remote display is fully operational. When HPD is asserted, the host system software will know to locate and configure the remote display.

3.2.4.2. DMC#

The DMC# signal is tied to ground on the Display-Mini Card to indicate that a Mini Card with DisplayPort capabilities is installed in the socket.

If implemented in the host platform, a host pull-up resistor in the range of 100 kΩ to 200 kΩ tied to no higher than +3.3Vaux is required on this pin.

3.2.4.3. MLDIR

The MLDIR signal indicates the functional direction of the DisplayPort data and auxiliary interfaces on a Mini Card; i.e. as a sink or source of the display-related interfaces.

Based on the specific DisplayPort capabilities of the Mini Card installed in the socket, the MLDIR signal termination on the card shall be as defined in Table 3-3.

Table 3-3: MLDIR Pin Termination

Display Capability on the Display-Mini Card	MLDIR Pin Termination on the Display-Mini Card
DisplayPort Sink; e.g., the card is a wireless display transmitter	Terminated directly to GND
DisplayPort Source; e.g., the card is a wireless display receiver	Terminated directly to +3.3Vaux
DisplayPort Sink or Source; e.g., the card is configurable as either a wireless display transmitter or receiver	Hi-Z (single input load)

For a Mini Card that offers bi-directional DisplayPort capabilities, the mechanism for configuring the direction of the display interface is application and/or product specific and not defined by this specification.

3.2.5. Auxiliary Signals

The auxiliary signals are provided on the system connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture, but may be required by specific implementations such as PCI Express Mini Card. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the +3.3Vaux supply, as it is the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with +3.3V. The use of the +3.3Vaux supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The PCI Express Mini Card add-in card and system connectors support the auxiliary signals described in the following sections.

3.2.5.1. Reference Clock

The REFCLK+/REFCLK- signals are used to assist the synchronization of the card's PCI Express interface timing circuits. Availability of the reference clock at the card interface may be gated by the CLKREQ# signal as described in Section 3.2.5.2~~3.2.5.2~~. When the reference clock is not available, it will be in the parked state. A parked state is when the clock is not being driven by a clock driver and both REFCLK+ and REFCLK- are pulled to ground by the ground termination resistors. Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional and tolerance requirements for the reference clock signals.

3.2.5.2. CLKREQ# Signal

The CLKREQ# signal is an open drain, active low signal that is driven low by the add-in card ~~PCI Express Mini Card function~~ to request that the PCI Express reference clock be available (active clock state) ~~in order~~ to allow the PCI Express interface to send/receive data. ~~-~~Operation of the CLKREQ# signal is determined by the state of the Enable Clock Power Management bit~~dynamic clock management enable bit~~ in the Link Control ~~R~~register ~~(offset 01000Ch)~~. When disabled, the CLKREQ# signal shall be asserted at all times whenever power is applied to the card, with the

Commented [TS3]: Per Base Spec Errata Rev 3.0, B17

exception that it may be de-asserted during L1 PM Substates. ~~-~~When enabled, the CLKREQ# signal may be de-asserted during an L1 Link state.

The CLKREQ# signal is also used by the L1 PM Substates mechanism. In this case, CLKREQ# can be asserted by either the system or add-in card to initiate an L1 exit. See the PCI Express Base Specification for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.

Commented [TS4]: ECN_L1_PM_Substates_with_CLKREQ_31_May_2013_Rev10a

Whenever dynamic clock management is enabled and when a card stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and module designs shall be tolerant of an active reference clock even when CLKREQ# is de-asserted by the module.

The card must drive this signal low during power up, whenever it is reset, and whenever it requires the reference clock to be in the active clock state. Whenever PERST# is asserted, including when the device is not in D0, CLKREQ# shall be asserted.

It is important to note that the PCI Express device must delay de-assertion of its CLKREQ# signal until it is ready for its reference clock to be parked. Also, the device must be able to assert its clock request signal, whether ~~or not~~ the reference clock is active or parked, when it needs to put its Link back into the L0 Link state. Finally, the device must be able to sense an electrical idle break on its up-stream-directed receive port and assert its clock request, whether ~~or not~~ the reference clock is active or parked.

The assertion and de-assertion of CLKREQ# are asynchronous with respect to the reference clock.

Add-in cards that do not implement a PCI Express interface shall leave this output unconnected on the card.

CLKREQ# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and other devices that may be powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the CLKREQ# signal network never causes damage to a component even if that ~~particular~~ component's power is not applied.

Additionally, the device must ensure that it does not pull CLKREQ# low unless CLKREQ# is being intentionally asserted in all cases, including when the related function is in $D3_{cold}$. This means that any component implementing CLKREQ# must be designed such that:

- Unpowered CLKREQ# output circuits are not damaged if a voltage is applied to them from other powered "wire-ORed" sources of CLKREQ#.
- When power is removed from its CLKREQ# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the CLKREQ# signal network continues to function properly when a mixture of powered and unpowered components have their CLKREQ# outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for CLKREQ#.

3.2.5.2.1. Power-up Requirements

CLKREQ# is asserted in response to PERST# assertion. On power up, CLKREQ# must be asserted by a PCI Express device within a delay (T_{PVCRL}) from the power rails achieving specified operating limits and PERST# assertion. This delay is to allow adequate time for the power to stabilize on the card and certain system functions to start prior to the card starting up. CLKREQ# may not be de-asserted while PERST# is asserted.

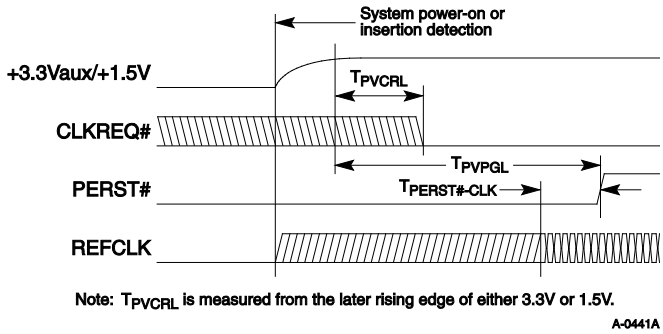


Figure 3-1: Power-Up CLKREQ# Timing

Table 3-4: Power-Up CLKREQ# Timings

Symbol	Parameter	Min	Max	Units
T_{PVCRL}	Power Valid to CLKREQ# Output active		100	µs
T_{PVPGL}	Power Valid to PERST# Input inactive	1		ms
$T_{PERST\#-CLK}$	REFCLK stable before PERST# inactive	100		µs

The system is required to have the reference clock for a PCI Express device in the parked clock state prior to device power-up. The state of the reference clock is undefined during device power-up, but it must be in the active clock state for a setup time $T_{PERST\#-CLK}$ prior to PERST# de-assertion.

3.2.5.2.2. Dynamic Clock Control

After a PCI Express device has powered up and whenever its upstream link enters the L1 link state, it shall allow its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts CLKREQ# (high) and it must allow that the reference clock will transition to the parked clock state within a delay (T_{CRHoff}).

To exit L1, the device must assert CLKREQ# (low) to re-enable the reference clock. After the device asserts CLKREQ# (low) it must allow that the reference clock will continue to be in the parked clock state for a delay (T_{CRLon}) before transitioning to the active clock state. The time that it

takes for the device to assert CLKREQ# and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of L1 recovery. This time must be ~~taken into account~~considered when the device is reporting its L1 exit latency.

When the PCI Express device supports and is enabled for Latency Tolerance Reporting (LTR), the device must allow that the reference clock transition to the active clock state may be additionally delayed by the system up to a maximum value consistent with requirements for the LTR mechanism. During this delay, the reference clock must remain parked. When exiting the parked state following the delay, the clock must be stable and valid within 400 ns.

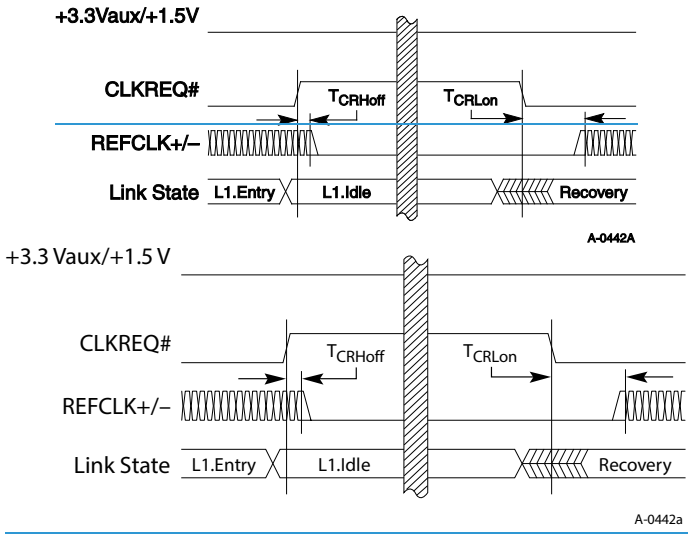


Figure 3-2: CLKREQ# Clock Control Timings

All links attached to a PCI Express device must complete a transition to the L1.Idle state before the device can de-assert CLKREQ#. The device must assert CLKREQ# when it detects an electrical idle break on any receiver port. The device must assert CLKREQ# at the same time it breaks electrical idle on any of its transmitter ports ~~in order~~ to minimize L1 exit latency.

Table 3-5: CLKREQ# Clock Control Timings

Symbol	Parameter	Min	Max	Units
T_{CRHoff}	CLKREQ# de-asserted high to clock parked	0		ns
T_{CRLon}	CLKREQ# asserted low to clock active		400*	ns

* T_{CRLon} is allowed to exceed this value when LTR is supported and enabled for the device.

There is no maximum specification for T_{CRHoff} and no minimum specification for T_{CRLon}. This means that the system is not required to implement reference clock parking or that the implementation may not always act on a device de-asserting CLKREQ#.

A device should also de-assert CLKREQ# when its link is in L2 or L3, much as it does during L1.

3.2.5.2.3. Clock Request Support Reporting and Enabling

Support for the CLKREQ# dynamic clock protocol ~~should~~ must be reported using the Clock Power Management bit ~~18~~ in the Link Capabilities register~~PCI Express link capabilities register (offset 0C4h)~~. ~~-~~To enable dynamic clock management, the Enable Clock Power Management bit ~~8~~ of the Link Control register is ~~(offset 010h) is~~ provided. By default, the card shall enable CLKREQ# dynamic clock protocol upon initial power up and in response to any warm reset by the host system. System software may subsequently disable this feature as needed. ~~See~~ Refer to the *PCI Express Base Specification*~~, Rev. 1.1 (or later)~~ for more information regarding these bits.

3.2.5.3. PERST# Signal

The PERST# signal is de-asserted to indicate when the system power sources are within their specified voltage tolerance and are stable. PERST# ~~should~~ must be used to initialize the card functions once power sources stabilize. PERST# is asserted when power is switched off and ~~also~~ can be used by the system to force a hardware reset on the card. The system may also use PERST# to cause a warm reset of the add-in card. Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the PERST# signal.

3.2.5.4. WAKE# Signal

PCI Express Mini Cards must implement WAKE# if the card supports either the wakeup function or the OBFF mechanism. ~~See~~ Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the WAKE# signal.

3.2.5.5. SMBus

The SMBus is a two-wire interface through which various system components can communicate with each other and the rest of the system. It is based on the principles of operation of I^2C. The SMBus interface pins are collectively optional for both the add-in card and system board. If the optional management features are implemented, SMBCLK and SMBDAT are both required. The pins assigned to these functions can only be used for these functions and are to be left disconnected if the functions are not implemented. See the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the SMBus.

3.2.6. Communications Specific Signals

3.2.6.1. Status Indicators

Three LED signals are provided to enable wireless communications add-in cards to provide status indications to users via system provided indicators.

LED_WPAN#, LED_WLAN#, and LED_WWAN# output signals are active low and are intended to drive system-mounted LED indicators. These signals shall be capable of sinking to ground a minimum of 9.0 mA at up to a maximum V_{OL} of 400 mV.

Table 3-6~~Table 3-6~~ presents a simple indicator protocol for each of two defined LED states as applicable for wireless radio operation. Although the actual definition of the indicator protocol is established by the OEM system developer, the following recommendation may be useful in establishing a minimum common implementation across many platforms.

Table 3-6: Simple Indicator Protocol for LED States

State	Definition	Interpretation
OFF	The LED is emitting no light.	Radio is incapable of transmitting. This state is indicated when the card is not powered, a wireless disable signal is asserted to disable the radio, or when the radio is disabled by software.
ON	The LED is emitting light.	Radio is capable of transmitting. The LED should remain ON even if the radio is not actually transmitting. For example, the LED remains ON during temporary radio disablements performed by the Mini Card of its own volition to do scanning, switching radios/bands, power-management, etc. If the card is in a state wherein it is possible that radio can begin transmitting without the system user performing any action, this LED should remain ON.

More advanced indicator protocols are allowed as defined by the OEM system developer. Advanced features might include use of blinking or intermittent ON states which can be used to indicate radio operations such as scanning, associating, or data transfer activity. Also, use of blinking states might be useful in reducing LED power consumption.

3.2.6.2. W_DISABLE# Signal

W_DISABLE1# and W_DISABLE2# are wireless disable signals that are provided for wireless communications add-in cards to allow users to disable, via a system-provided switch, the add-in card's radio operation ~~in order~~ to meet public safety regulations or when otherwise desired. Implementation of this signal is required for systems and all add-in cards that implement radio frequency capabilities. Multiple wireless disable signals are provided to ease managing multiple radios on a single add-in card. If only one wireless disable signal is implemented by the system, asserting that single signal ~~should~~ must be used for collectively disabling all radios on the add-in card.

The wireless disable signals are active low signals that when asserted (driven low) by the system shall disable radio operation. When implemented, a pull-up resistor between each wireless disable signal and +3.3Vaux is required on the card and should be in the range of 100 kΩ to 200 kΩ. The assertion and de-assertion of each wireless disable signal is asynchronous to any system clock. All transients resulting from mechanical switches need to be de-bounced by system circuitry.

When a wireless disable signal is asserted, all ~~of~~ the radios associated with that signal shall be disabled. When a wireless disable signal is not asserted, the associated radios may transmit if not

disabled by other means such as software. These signals may be shared between multiple Mini Cards.

In normal operation, the card should disassociate with the wireless network and cease any further operations (transmit/receive) as soon as possible after the wireless disable signal is asserted. Given that a graceful disassociation with the wireless network fails to complete in a timely manner, the Mini Card shall discontinue any communications with the network and assure that its radio operation has ceased no later than 30 seconds following the initial assertion of the wireless disable signal. Once the disabling process is complete, the LED specific to the radio shall indicate the disabled condition to the user.

The card should initiate and indicate to the user the process of resuming normal operation within one second of de-assertion of the wireless disable signal. Due to the potential of a software disable state, the combination of both the software state and wireless disable signal assertion state must be determined before resuming normal operation. Table 3-7 illustrates this requirement as a function of wireless disable signal and the software control setting such that the radio's RF operation remains disabled unless both the hardware and software are set to enable the RF features of the card.

Table 3-7: Radio Operational States

Wireless Disable Signal	SW Control Setting*	Radio Operation
De-asserted (HIGH)	Enable Radio	Enabled (RF operation allowed)
De-asserted (HIGH)	Disable Radio	Disabled (no RF operation allowed)
Asserted (LOW)	Enable Radio	Disabled (no RF operation allowed)
Asserted (LOW)	Disable Radio	Disabled (no RF operation allowed)

* This control setting is implementation specific; this column represents the collective intention of the host software to manage radio operation.

The system is required to assure that each wireless disable signal be in a deterministic state (asserted or de-asserted) whenever power is applied to the add-in; i.e., +3.3Vaux is present.

3.2.7. User Identity Module (UIM) Interface

The UIM signals are defined on the system connector to provide the interface between the removable User Identity Module (UIM), an extension of a Subscriber Identity Module (SIM), and a wireless wide area network (WWAN) radio device residing on the PCI Express Mini Card add-in card. The UIM contains parameters necessary for the WWAN device's operation in a wireless wide area network radio environment. The UIM signals are described in the following sections for PCI Express Mini Card add-in cards that support the off-card UIM interface.

3.2.7.1. UIM_PWR

Refer to ISO/IEC 7816-3 for more details on the voltage and current tolerance requirements for the UIM_PWR power source. Note that the UIM grounding requirements can be provided by using any GND pin. Only PCI Express Mini Card add-in cards that support a UIM card shall connect to this pin. If the add-in card has UIM support capabilities, it must support the UIM_PWR power source at the appropriate voltage for each class of operating conditions (i.e., voltage) supported as defined in ISO/IEC 7816-3.

UIM_PWR maps to contact number C1 as defined in ISO/IEC 7816-2.

3.2.7.2. UIM_RESET

This signal provides the UIM card with the reset signal. Refer to ISO/IEC 7816-3 for more details on the functional and tolerance requirements for the UIM_RESET signal. Only PCI Express Mini Card add-in cards that support a UIM card shall connect to this pin.

UIM_RESET maps to contact number C2 as defined in ISO/IEC 7816-2.

3.2.7.3. UIM_CLK

This signal provides the UIM card with the clock signal. Refer to ISO/IEC 7816-3 for more details on the functional and tolerance requirements for the UIM_CLK signal. Only PCI Express Mini Card add-in cards that support a UIM card shall connect to this pin.

UIM_CLK maps to contact number C3 as defined in ISO/IEC 7816-2.

3.2.7.4. UIM_SPU

This signal is available for either standard or proprietary use, as input and/or output. Refer to ISO/IEC 7816-3 for more details on the voltage and current tolerance requirements for the UIM_SPU signal.
UIM_SPU maps to contact number C6 as defined in ISO/IEC 7816-2.

3.2.7.5. UIM_DATA

This signal is used as output (UIM reception mode) or input (UIM transmission mode) for serial data. Refer to ISO/IEC 7816-3 for more details on the functional and tolerance requirements for the UIM_DATA signal. Only PCI Express Mini Card add-in cards that support a UIM card shall connect to this pin.

UIM_DATA maps to contact number C7 as defined in ISO/IEC 7816-2.

3.2.7.6. UIM_IC_DP

This signal is used as the Inter-Chip USB D+ Data line.

Refer to ~~"~~ the Inter-*Chip USB supplement to the USB 2.0 Specification*~~"~~ ~~-~~and ETSI TS 102 600 for the functional and tolerance requirements for this signal.

Only PCI Express Mini Card add-in cards that support a UIM card ~~shall~~ must connect to this pin.
UIM_IC_DP maps to contact number C4 as defined in ISO/IEC 7816-2.

3.2.7.7. UIM_IC_DM

This signal is used as the Inter-Chip USB D- Data line.

Refer to ~~"~~*Inter-Chip USB supplement to the USB 2.0 Specification*~~"~~ and ETSI TS 102 600 for the functional and tolerance requirements for this signal.

Only PCI Express Mini Card add-in cards that support a UIM card ~~shall~~ must connect to this pin. UIM_IC_DM maps to contact number C8 as defined in ISO/IEC 7816-2.

3.3. Connector Pin-out Definitions

The following sections illustrate signal pin-outs for the system connector. Table 3-8~~Table 3-8~~ lists the pin-out for both the 52-pin and the 76-pin system connectors. For the 52-pin version of the connector, pins 53-76 are not present.

Table 3-8: System Connector Pin-out

Pin #	Name	Pin #	Name
75	GND	76	MLDIR
73	ML0p	74	GND
71	ML0n	72	GND
69	GND	70	ML1p
67	GND	68	ML1n
65	ML2p	66	GND
63	ML2n	64	GND
61	GND	62	ML3p
59	GND	60	ML3n
57	AUXp	58	GND
55	AUXn	56	GND
53	DMC#	54	HPD
Mechanical Key			
51	W_DISABLE2#	52	+3.3Vaux
49	Reserved	50	GND
47	~~Reserved~~ANTCTRL3	48	+1.5V/ ANTCTRL1
45	ANTCTRL2~~Reserved~~	46	LED_WPAN#
43	GND	44	LED_WLAN#
41	+3.3Vaux	42	LED_WWAN#
39	+3.3Vaux	40	GND
37	GND	38	USB_D+
35	GND	36	USB_D-
33	PETp0 or SSTX+	34	GND
31	PETn0 or SSTX-	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V/ ANTCTRL0
25	PERp0 or SSRX+	26	GND
23	PERn0 or SSRX-	24	+3.3Vaux

Commented [TS5]: Per Combined Antenna Tuning/Coexistence Signal ECN

Commented [TS6]:

Commented [TS7R6]: Per Combined Antenna Tuning/Coexistence Signal ECN

Pin #	Name	Pin #	Name
21	GND	22	PERST#
19	UIM_IC_DP	20	W_DISABLE1#
17	UIM_IC_DM	18	GND
Mechanical Key			
15	GND	16	UIM_SPU
13	REFCLK+	14	UIM_RESET
11	REFCLK-	12	UIM_CLK
9	GND	10	UIM_DATA
7	CLKREQ#	8	UIM_PWR
5	COEX2	6	1.5V/COEX3
3	COEX1	4	GND
1	WAKE#	2	3.3Vaux

Commented [TS8]: Per Combined Antenna Tuning/Coexistence Signal ECN

3.3.1. Grounds

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving ground (GND) pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ground planes within a card design.

3.3.2. Coexistence Pins

COEX1, ~~and~~ COEX2, and COEX3 are provided to allow for the implementation of wireless coexistence solutions between the radio(s) on the Mini Card and other off-card radio(s). These other radios can be located on another Mini Card located in the same host platform or as alternate radio implementations (e.g., using a PCI Express Mini CEM or a proprietary form-factor add-in solution).

Commented [TS9]: Per Combined Antenna Tuning/Coexistence Signal ECN

The functional definition of these pins ~~are~~ is OEM specific and should be coordinated between the host platform OEM and card vendors. The ordered labeling of these signals in this specification ~~are~~ is intended to help establish consistent implementations, where practical, across multiple instances of cards in the host platform. ~~Per Combined Antenna Tuning/Coexistence Signal ECN,~~ Note that COEX3 is shared with a 1.5 V pin (see ~~s~~Section 3.2.1)

Commented [TS10]: Per Combined Antenna Tuning/Coexistence Signal ECN

3.3.3. Reserved Pins

Reserved pins are expected to be not terminated on either the add-in card or system board side of the connector. These pins are reserved for definition with future revisions of this specification. Non-standard use of these pins may result in incompatibilities in solutions aligned with the future revision.

3.3.4. Tunable Antenna Pins

Pins ANTCTRL[3:0] define a 4-pin interface for allowing on-board radio(s) to tune antennas external to the Mini Card. This interface is typically used when the external antenna subsystem needs to have knowledge of the frequency that the on-board radio(s) are operating on ~~in order~~ to achieve peak performance.

The functional definition of these pins, including voltage levels and protocol, ~~are~~is OEM specific. Up to ~~4~~four pins ~~may be~~are used in some implementations, while other implementations ~~will~~ use only a subset of the pins defined. The purpose of including them in this specification is to avoid non-standard pin assignments for this interface and to have a consistent naming scheme across the industry.

ANTCTRL0 and ANTCTRL1 are sharing functionality with 1.5V pins, whether the add-in card is using these pins for 1.5V or tunable antennas is OEM-specific and shall be documented by the OEM.

Commented [TS11]: Per Combined Antenna Tuning/Coexistence Signal ECN

3.4. Electrical Requirements

3.4.1. Logic Signal Requirements

The 3.3V card logic levels for single-ended digital signals (WAKE#, CLKREQ#, PERST#, W_DISABLE1#, W_DISABLE2#, and MLDIR) are given in Table 3-9.

Table 3-9: DC Specification for 3.3V Logic Signaling

Symbol	Parameter	Conditions	Min	Max	Units	Notes
+3.3Vaux	Supply Voltage		3.3 - 5%	3.3 + 9%	V	3
V_{IH}	Input High Voltage		2.0	3.6	V	1
V_{IL}	Input Low Voltage		-0.5	0.8	V	1
I_{OL}	Output Low Current for open-drain signals	0.4 V	4		mA	2
I_{IN}	Input Leakage Current	0 V to 3.3 V	-10	+10	µA	1
I_{LKG}	Output Leakage Current	0 V to 3.3 V	-50	+50	µA	1
C_{IN}	Input Pin Capacitance			7	pF	1
C_{OUT}	Output Pin Capacitance			30	pF	2
$R_{PULL-UP}$	Pull-up resistance		9	60	kΩ	4

Commented [TS12]: ECN_L1_PM_Substates_with_CLKREQ_31_May_2013_Rev10a

Notes:
1. Applies to PERST#, W_DISABLE1#, W_DISABLE2#, MLDIR (when applicable), and WAKE# (when used for OBFF signaling), and CLKREQ# (when used for L1 exit signaling).
2. Applies to CLKREQ# and WAKE#.
3. As measured at the card connector pad.
4. Applies to CLKREQ# pull-up on host system.

Commented [TS13]: ECN_L1_PM_Substates_with_CLKREQ_31_May_2013_Rev10a

3.4.2. Digital Interfaces

Signal integrity requirements are defined separately for 2.5 ~~Gbps~~ GT/s and 5.0 ~~Gbps~~ GT/s applications. Mini Card sockets that are designed for 5.0 ~~Gbps~~ GT/s applications shall also be useable with Mini Cards that only operate up to 2.5 ~~Gbps~~GT/s.

3.4.2.1. Signal Integrity Requirements and Test Procedures for 2.5 GT/s Support

A common electrical test fixture is specified and used for evaluating connector signal integrity. The test fixture has 50 Ω single ended traces 0.1524 mm (6 mils) wide that must be uncoupled. The impedance variation of those traces shall be controlled within ±5%. Refer to Appendix A for detailed discussions on the test fixture.

Detailed testing procedures, such as the vector network analyzer settings, operation, and calibration are specified in Appendix A. This appendix should be used in conjunction with the PCI Express Connector Test Fixture.

For the insertion loss and return loss tests, the measurement shall include 1-inch long PCB traces with 0.5 inches on the system board and 0.5 inches on the add-in card. Note that the edge finger pad is not counted as the add-in card PCB trace. It is considered part of the connector interface. The 1-inch PCB trace included in the connector measurement is a part of the trace length allowed on the system board.

Either single ended measurements that are processed to extract the differential characteristics or true differential measurements are allowed. The detailed definition and description of the test fixture and the measurement procedures are provided separately in Appendix A.

An additional consideration to the connector electrical performance is the connector-to-system board and connector-to-add-in-card launches. The connector through-hole pad and anti-pad sizes, as well as trace layout on the system board shall follow the recommendations in the *PCI Express Electrical Design Guidelines*. On the add-in card, the ground and power planes underneath the PCI Express high-speed signals (edge fingers) shall be removed. Otherwise, the edge fingers will have too much capacitance and greatly degrade the connector performance. More detailed discussion on the add-in card electrical design can be found in Appendix A and *PCI Express Electrical Design Guidelines*.

Table 3-10~~Table 3-10~~ lists the electrical signal integrity parameters, requirements, and test procedures.

Table 3-10: Signal Integrity Requirements and Test Procedures for 2.5 GT/s

Parameter	Procedure	Requirements
Differential Insertion loss (DDIL)	EIA 364-101 The EIA standard must be used with the following considerations: 1. The step-by-step measurement procedure is outlined in Appendix A. 2. A common test fixture for connector characterization will be used. 3. This is a differential insertion loss requirement. Therefore, either true differential measurement must be made or post processing of the single ended measurements must be done to extract the differential characteristics of the connector. The methodology of doing so is covered in Appendix A.	≤1 dB up to 1.25 GHz ≤ [1.6 * (f - 1.25)+1] dB for 1.25 GHz < f ≤ 3.75 GHz (for example, ≤5 dB a 3.75 GHz)
Differential Return loss (DDRL)	EIA 364-108 The EIA standard must be used with the following considerations: 1. The step-by-step measurement procedure is outlined in Appendix A. 2. A common test fixture for connector characterization will be used. 3. This is a differential return loss requirement. Therefore, either true differential measurement must be made or post processing of the single ended measurements must be done to extract the differential characteristics of the connector. The methodology of doing so is covered in Appendix A.	≤ -12 dB up to 1.3 GHz; ≤ -7 dB for 1.3 GHz < f ≤ 2 GHz; ≤ -4 dB for 2 GHz < f ≤ 3.75 GHz
Intra-pair skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max

Parameter	Procedure	Requirements
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. This is reflected in the measurement procedure and adjustments to the procedure should be made accordingly. 2. The step-by-step measurement procedure is outlined in Appendix A. 3. A common test fixture for connector characterization will be used. This is a differential crosstalk requirement between a victim differential signal pair and all ~~of~~ its adjacent differential signal pairs. Therefore, either true differential measurement must be made or post processing of the single ended measurements must be done to extract the differential crosstalk of the connector. The methodology of doing so is covered in Appendix A.	≤ -32 dB up to 1.25 GHz; ≤ -[32 - 2.4 * (f - 1.25)] dB for 1.25 GHz < f ≤ 3.75 GHz (for example, ≤ -26 dB at f = 3.75 GHz)
Jitter	By design; measurement not required	10 ps max

Notes:

1. A network analyzer is preferred. If greater dynamic range is required, a signal generator/spectrum analyzer may be used. Differential measurements require the use of a two-port (or a four-port) network analyzer to measure the connector. The differential parameters may be measured directly if the equipment supports “True” differential excitation. (“True” differential excitation is the simultaneous application of a signal to one line of the pair and a 180-degree phase shifted version of the signal to the second line of the pair.) If single ended measurements are made, the differential connector parameters must be derived from the single ended measurements as defined in Appendix A.
2. If differential measurements are made directly by application of differential signals, the equipment must use phase-matched fixturing. The fixturing skew and measurement cabling should be verified to be < 1 ps on a TDR.
3. The connector shall be targeted for a 100 Ω differential impedance, though it is not explicitly specified.

3.4.2.2. Signal Integrity Requirements and Test Procedures for 5.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects, not including the connector via, are de-embedded from measurements. Test fixture requirements and recommendations are also included in this section.

Table 3-11 lists the electrical signal integrity parameters, requirements, and test procedures.

~~3.4.2.2. Signal Integrity Requirements and Test Procedures for 5.0 GT/s Support~~

~~An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects, not including the connector via, are de-embedded from measurements. Test fixture requirements and recommendations are also included in this section.~~

~~Table 3-11 lists the electrical signal integrity parameters, requirements, and test procedures.~~

Table 3-11: Signal Integrity Requirements and Test Procedures for 5.0 GT/s

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 ~~ohm~~ Ohm differential impedance. 2. The test fixture shall meet the test fixture requirement defined later in this section. The test fixture effect shall be removed from the measured S parameters. ~~Refer~~ See to Note 1.	≥ -0.5 dB up to 2.5 GHz; ≥ -[0.8*(f-2.5)+0.5] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥-2.5 dB at f = 5 GHz); ≥ -[3.0*(f-5)+2.5] dB for 5 GHz < f ≤ 7.5 GHz (for example, ≥-10 dB at f = 7.5 GHz);
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 O~~o~~hms differential impedance. 2. The test fixture shall meet the test fixture requirement in further in this section. The test fixture effect shall be removed. ~~Refer~~ See to Note 1.	≤ -15 dB up to 3.0 GHz; ≤ -5 dB for 3.0 GHz < f ≤ 5 GHz; ≤ -1 dB for ~~-~~5.0 GHz < f ≤ 7.5 GHz.
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max

Parameter	Procedure	Requirements
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. This is a differential crosstalk requirement between a victim differential signal pair and all ~~of~~ its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 ~~o~~Ohm differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for 2.5 GHz < f ≤ 5.0 GHz; ≤ -20 dB for 5.0 GHz < f ≤ 7.5 GHz;

Notes:
1. The specified S parameters requirements are for connector only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.

The test fixture for connecter S-parameter measurement should be designed and built to the following requirements:

- The test fixture shall be an FR4-based PCB of the micro-strip structure; the dielectric thickness or stack-up shall be approximately 102 mm (4 mils).
- The total thickness of the test fixture PCB shall be 1.57 mm (0.62") and the test add-in card should be a break-out card fabricated in the same PCB panel for the fixture.
- The measurement signals shall be launched into the connector from the top of the test fixture, capturing the through-hole stub effect.
- Traces between the connector and measurement ports (SMA or microprobe) should be uncoupled.
- The trace lengths between the connector and measurement port shall be minimized. The maximum trace length shall not exceed 45.72 mm (1800 mils). The trace lengths between the connector and measurement port on the test baseboard and add-in card shall be equal. Note that the edge finger pad is not counted as the add-in card PCB trace; it is considered as a part of the connector interface.
- All of the traces on the test board and add-in card must be held to a characteristic impedance of 50 Ohms with a tolerance of +/- 7%.
- The test add-in card edge finger pads shall be fabricated per mechanical requirements defined in this specification. The ground plane immediately underneath the edge finger pads must be removed.
- The through-hole on the test board shall have the following stack-up: .711 mm (28 mil) finished hole, 1.067 mm (42 mil) pad, and 1.473 mm (58 mil) anti-pad.
- Use of SMA connectors is recommended. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 60 ps rise time is recommended to be within 50+/-7 ohms.

If a fixture with other characteristics is used, the fixture effects must be reliably removed and must not impact measurement accuracy.

3.4.3. Power

PCI Express Mini Card has two defined power rails: +3.3Vaux and +1.5V (optional). Table 3-12~~Table 3-12~~ lists the voltage tolerances and power ratings for each PCI Express Mini Card slot implemented in a system.

Table 3-12: Power Ratings

Power Rail	Voltage Tolerance	D0-D2, $D3_{hot}$ Power[1]		$D3_{cold}$ Power[2, 3]	
		Peak (max) mA	Normal (max) mA	Peak (max) mA	Normal (max) mA
3.3Vaux	+9% -5%	2,750	1,100	2,750 (wake enabled)	250 (wake enabled) 5 (no wake enabled)
+1.5V	±5%	500	375	N/A	N/A

1. For USB: Power states greater than Bus Suspend.
2. For USB: Wake enabled is USB Remote ~~wakeup~~Wakeup-Enabled and No Wake enabled is USB Remote ~~wakeup~~Wakeup-Disabled.
3. This D3 current limit only applies when the +1.5V voltage source is not available; i.e., the card is in $D3_{cold}$.

Definitions:
Peak – The highest averaged current value over any 100-microsecond period
Normal – The highest averaged current value over any 1-second period

Note: For Peak, the value of "100-microsecond period" was derived as follows:
The period~~ ~~of~~ ~~time that the current is to be measured and averaged over must be less than a single GPRS slot time. This enables measurement of the average peak current within a single GPRS slot. ~~ ~~There are 4.6 milliseconds/GPRS frame and eight slots per GPRS frame = 575 microseconds/slot. ~~ ~~The 100-microsecond period < 575-microsecond period.

The operation of the +3.3Vaux power source shall conform to the *PCI Bus Power Management Interface Specification* and the *Advanced Configuration and Power Interface (ACPI) Specification*, except as otherwise specified by this document. If the host does not support wake from D3, +3.3Vaux ~~may be~~is removed by the host when +1.5V (if supported) is removed.

3.5. Card Enumeration

All PCI Express-based Mini Cards must enumerate to either multi-function or single function PCI Endpoints.

All USB-based Mini Cards must enumerate to either single function traditional USB Devices or Composite Devices or Compound Devices.

All DisplayPort-based Mini Cards must enumerate to either a Sink or Source Device consistent with MLDIR pin termination or logic state for configurable cards. Optionally, a Display-Mini Card may support either (or both) PCI Express or USB interfaces in addition to its DisplayPort interface.

A

A. Supplemental Guidelines for PCI Express Mini Card Connector Testing

This section provides supplemental guidelines for testing a PCI Express Mini Card connector. Because the PCI Express Mini Card connector has a different form factor and pin configuration than the desktop connector, a set of specific test boards has been designed to be used as the test vehicle for the PCI Express Mini Card connectors.

A.1. Test Boards Assembly

There are three test boards: a baseboard and two plug-in cards. The baseboard has the footprints for the PCI Express Mini Card connector. One plug-in card is used in insertion loss and return loss measurement. The other plug-in card is used for crosstalk testing.

A.1.1. Base Board Assembly

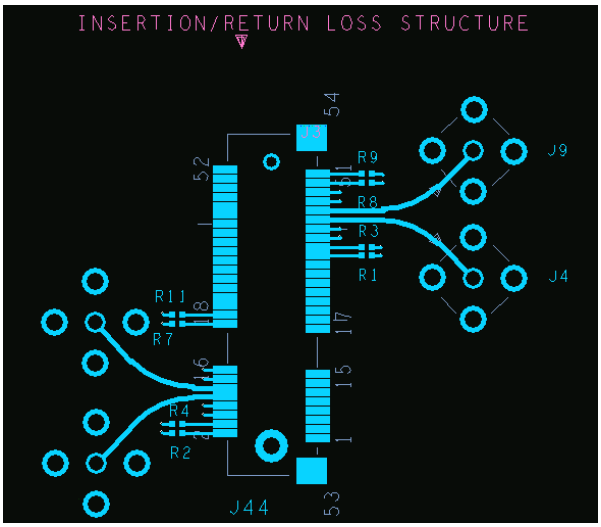


Figure A-1: Base Board Insertion Loss/Return Loss Structure

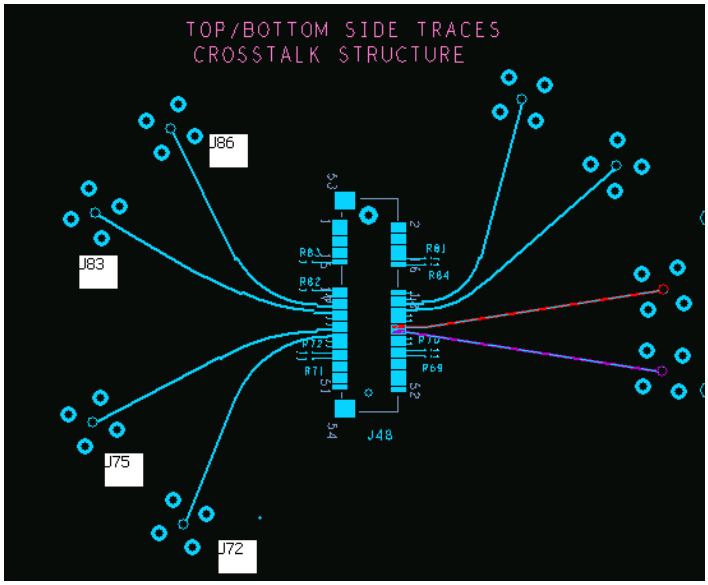


Figure A-2: Base Board Crosstalk Structure

All parts should be on the front side of the baseboard (i.e., the side printed with description of the board). Load the PCI Express Mini Card connector to location J44 and J48. Load female SMA connectors to locations J4, J9, J72, J75, J83, and J86. Load 0402-SMT 50 Ω resistors to locations R1, R3, R8, R9, R71, R72, R82, and R83.

A.1.2. Plug-in Cards Assembly

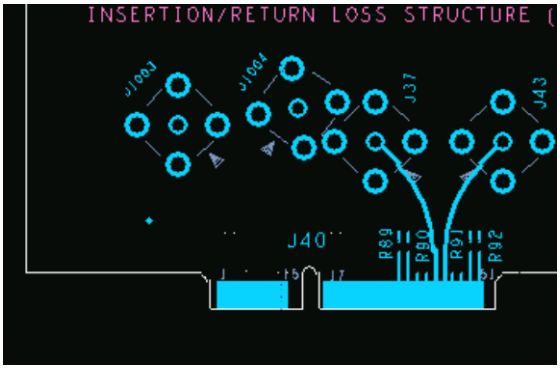


Figure A-3: Plug-in Card Insertion Loss/Return Loss Structure

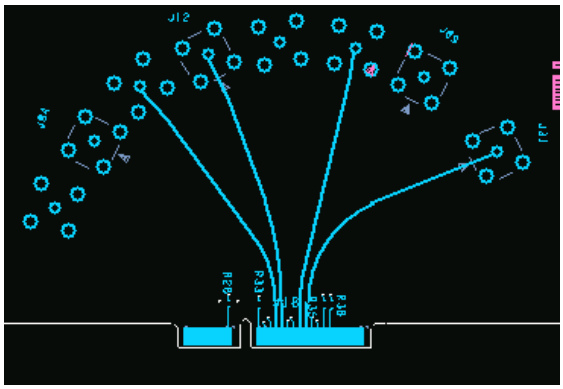


Figure A-4: Plug-in Card Insertion Loss/Return Loss Structure

All parts should be on the front side of the baseboard (i.e., the side printed with description of the board). Load female SMA connectors to locations J37, J43, J12, J31, J8, and J22. Load 0402-SMT 50 Ω resistors to locations R89, R90, R91, R92, R28, R33, R35, and R38.

A.2. Insertion Loss Measurement

Follow the guidelines in Section 5 of the *PCI Express Connector High Speed Electrical Test Procedure*. The mobile test vehicle has the test structures (SMA and traces) as shown in Figure A-1~~Figure A-1~~ and Figure A-3~~Figure A-3~~.

A.3. Return Loss Measurement

Follow the guidelines in Section 6 of the *PCI Express Connector High Speed Electrical Test Procedure*. The mobile test vehicle has the test structures (SMA and traces) as shown in Figure A-2~~Figure A-2~~ and Figure A-4~~Figure A-4~~.

A.4. Near End Crosstalk Measurement

Because the PCI Express Mini Card connector is x1 (one transmit differential pair and one receive differential pair), the near end crosstalk measurement can be limited to the two differential pairs. Therefore, the test structure and the mathematics of calculating the near end crosstalk are simplified. The SMA connectors on the board shown in Figure 4 of the *PCI Express Connector High Speed Electrical Test Procedure* can be reduced to the following: J72, J75, J83, and J86. Other neighboring pins on the connector are terminated to 50 Ω or ground. J72 and J75 form the aggressor pair and J83 and J86 form the victim pair.

Figure A-5~~Figure A-5~~ shows the configuration used in mobile measurements followed by an equation to calculate the near end crosstalk. For details on making measurements, refer to Section 7 of the *PCI Express Connector High Speed Electrical Test Procedure*.

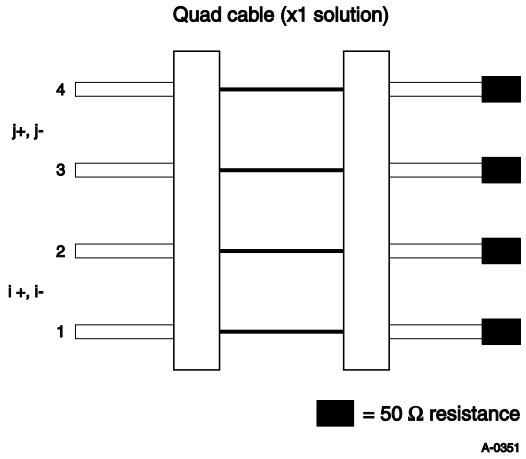


Figure A-5: Near End Crosstalk Measurement Illustration

$$DDNEXT = \frac{1}{2}\left(S_{4\_1} + S_{3\_2}\right) - \frac{1}{2}\left(S_{3\_1} + S_{4\_2}\right)$$

Equation A-1: Simplified NEXT Equation for Mobile

Follow the procedures in Section 8 of the *PCI Express Connector High Speed Electrical Test Procedure* to measure the S-parameters. As a result, substituting the reference designator (J numbers) into Equation A-1, we have:

$$DDNEXT = \frac{1}{2}\left(S_{72\_83} + S_{75\_86}\right) - \frac{1}{2}\left(S_{75\_83} + S_{72\_86}\right)$$

Equation A-2: NEXT Equation for Mobile Connector

B

B. I/O Connector Guidelines

This appendix provides supplemental guidelines regarding available I/O connectors that have been successfully used for applications intended for PCI Express Mini Card.

B.1. Wire-line Modems

I/O connector recommendations for wire-line modem applications are provided in Section 5.5.2 of the *Mini PCI Specification~~, Revision 1.0~~*.

B.2. IEEE 802.3 Wired Ethernet

For I/O connector recommendations for IEEE 802.3 wired Ethernet (LAN) applications, refer to Section 5.5.2 of the *Mini PCI Specification~~, Revision 1.0~~*.

B.3. IEEE 802.11 Wireless Ethernet

The following commercially-available connectors have been successfully used in Mini PCI wireless applications. Refer to vendor specifications for more information.

Hirose U.FL Series – SMT Ultra-Miniature Coaxial Connectors (www.hirose.com)